Time: 3 Hours **Max Marks: 80**

N.B. **1) Question No.1 is compulsory**
2) Solve any three questions from the remaining questions.
3) Assume suitable data if necessary.

1		**Solve any four of the following**	**20**
	(a)	Compare Bus based approach SoC and NoC	
	(b)	Illustrate all types of Pipeline Hazards	
	(c)	State ways to reduce data dependencies	
	(d)	Explain the basic SoC model with a neat diagram	
	(e)	Explain Virtual Component Interface (VCI)	
2	(a)	Explain the memory address translation mechanism in caches, explain the concept of TLB in translation	**10**
	(b)	With respect to cache organizations explain the multilevel cache systems and limits on cache size	**10**
3	(a)	With respect to interconnects Explain the NoC based approach and its advantages over the bus-based approach	**10**
	(b)	Explain the AMBA and core connect interconnect strategies, also elaborate on which interconnect strategy is suitable for what application	**10**
4	(a)	What is the superscalar processor, explain with diagram and explain an application of the superscalar processor	**10**
	(b)	With a detailed diagram explain the pipelined architecture of processor	**10**
5	(a)	Explain the design trade-off triangle, how does it apply to SoC	**10**
	(b)	What are reconfigurable processors and instructions	**10**
6		Write short notes on <u>any **Four**</u>.	**20**

I. Vectored Processors
II. Cache Write Policies
III. Processor Selection Criteria
IV. Bus Arbitration
V. eDRAM for SoC
