Duration: 3 Hours **Total Marks: 80**

Note:

1) **Question No 1 is Compulsory.**
2) **Answer any three from the remaining questions.**
3) **Assume suitable data wherever required**

Q1. Solve any four of the following. **(20)**

a. Explain Oxide related capacitances in MOSFET.

b. Write a short note on power dissipation in CMOS circuits.

c. Implement the function F= $\overline{(A+B+C).(DE)}$ using standard CMOS logic

d. Implement 4 X 4 NAND based ROM array.

e. Write short on High-speed adders.

Q2.a Explain Constant Voltage and Constant Field Scaling in detail with their advantages and disadvantages. **(10)**

b. Explain CMOS inverter characteristics mentioning all regions of operation. **(10)**

Q3.a Compare Pass transistor logic, NMOS logic and CMOS logic. **(10)**

b. Compare SRAM with DRAM. Draw 6T SRAM Cell and explain its read and write operations **(10)**

Q4.a Compare Static CMOS and Pseudo NMOS design styles. Implement 2 input NOR gate using pseudo NMOS design style. **(10)**

b. Calculate noise margin of a CMOS inverter with the given parameters: **(10)**
NMOS $V_{TO,n}$ =0.6V, u_nC_{ox} = 60 uA/V^2, (W/L)n = 8,
PMOS $V_{TO,p}$ = -0.7V, u_pC_{ox} = 25 uA/V^2, (W/L)p = 12,
V_{DD} = 3.3 V.

Q5.a Draw D flip flop using CMOS logic and explain the working. **(10)**

b. Draw Carry Look Ahead Adder chain using Dynamic CMOS Logic. **(10)**

Q6. Explain any four **(20)**

a. BJT and MOS Technologies

b. Noise Margin

c. Sense Amplifier

d. 4 X 4 Barrel Shifter

e. ZIPPER logic design style

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