University of Mumbai
Examination Summer 2022

Program: BE Electronics Engineering

Program No.: 1T01136

Name of the Examination:T.E. (Electronics Engineering) (SEM-VI)

(Choice Base Credit Grading System) (R- 19) (C Scheme)

Subject (Paper Code) :89368 / / Digital Design with Reconfigurable Architecture (DLOC)

Time: 2-hour 30 min **Max. Marks: 80**

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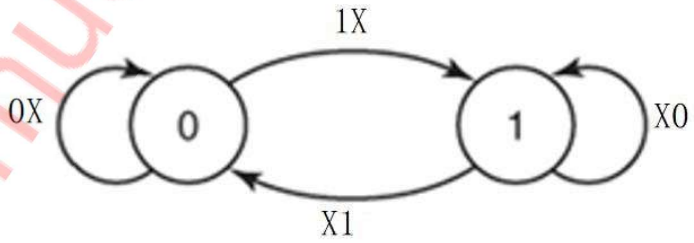
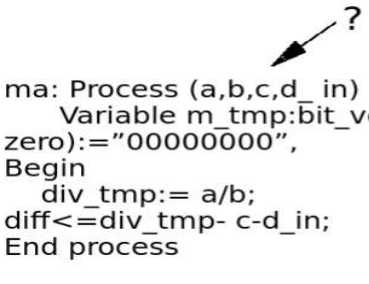
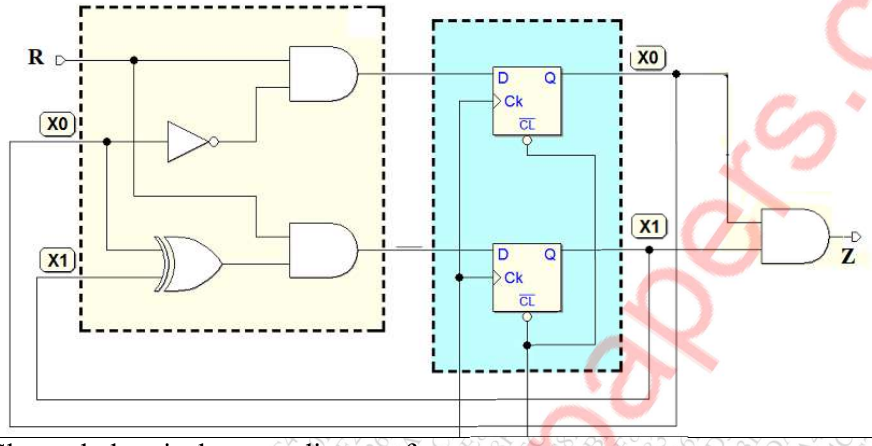
Note:- Choose the correct option for the following questions. All the questions are compulsory and carry equal marks.	
Q1.	If the declarative part in the architecture of a half adder is as below, identify the type of architecture. component XOR2 port (X,Y:in BIT, z: out BIT); end component; component AND2 port (L,M:in BIT, z:out BIT); end component;
Option A:	behavioral
Option B:	structural
Option C:	dataflow
Option D:	mixed Design
Q2.	Which flipflop does possess the following state diagram? 
Option A:	JK flip flop
Option B:	T flip flop
Option C:	SR flip flop
Option D:	D flip flop

Q3.	Which Method is not a State Reduction Technique?
Option A:	Implication Chart Method
Option B:	Inspection Method
Option C:	Partition Method
Option D:	One-Hot Encoding Method
Q4.	***process (clk)*** ***variable A,B,C,D: std_logic:= '0';*** ***begiin*** ***if clk'event and clk='1' then*** ***A <= Sin:*** ***B <= A;*** ***C <= B;*** ***D <= C;*** ***end if;*** ***Pout <= A&B&C&D;*** ***end process*** In the above code, if input signal Sin = '1' then at the end of 1 cycle at clk, the output Pout will be……..
Option A:	0001
Option B:	0000
Option C:	1000
Option D:	1111
Q5.	Which among the following state machine notations are generated outside the sequential state machine?
Option A:	Input variables
Option B:	Output variables
Option C:	State variables
Option D:	Excitation variables
Q6.	In VHDL an attribute, S ' LAST_EVENT returns …...
Option A:	Boolean value TRUE or FALSE
Option B:	Bit '1' or '0'
Option C:	Last value of S
Option D:	the time since the last event on signal S
Q7.	Which of the following is the correct sequence of steps of Digital design with FPGA?
Option A:	Design Entry, Mapping, Place and route, Simulation, Bit stream generation, Synthesize
Option B:	Design Entry, Simulation, Synthesize, Mapping, Place and route, Bit stream generation
Option C:	Bit stream generation, Design Entry, Simulation, Synthesize, Mapping, Place and route
Option D:	Simulation, Synthesize, Design Entry, Place and route, Mapping, Bit stream generation

Q8.	What does an arrow indicate in the schematic format of process statement given below? 
Option A:	Variable declaration
Option B:	Process body
Option C:	Process label
Option D:	Sensitivity List
Q9.	Characteristic equation of J-K flipflop is……..
Option A:	$Q_{n+1} = Q'_nJ + Q_nK'$
Option B:	$Q_{n+1} = Q_nJ + Q'_nK'$
Option C:	$Q_{n+1} = Q_nJ' + Q_nK$
Option D:	$Q_{n+1} = Q'_nJ' + Q_nK$
Q10.	Which mode in VHDL allows to make the signal assignments to an output port while preventing it from reading?
Option A:	IN
Option B:	INOUT
Option C:	OUT
Option D:	BUFFER

Q.2	**Answer any Two questions out of Three** **(10 marks each)**
A	Write a VHDL code that divides the Clock frequency by 10.
B	i)Write a VHDL code of T flipflop. ii)Using T flipfop as a component write a code for 4 bit asynchronous counter.
C	Write a VHDL code for serial adder.

Q.3	**Solve any two questions out of Three** **(10 marks each)**
A	Write short notes on the following: i) Clock management in FPGA. ii) Operators used in VHDL with examples
B	i) Explain Booth Multiplication with example. ii)Write a VHDL code for Booth's multiplier.
C	Explain SRAM based FPGA architecture in detail.

Q.4	**Answer any Two questions out of Three** **(10 marks each)**
A	Design a Mealy sequence detector circuit to detect an overlapping sequence "10110" using D flip flop and logic gates.
B	Analyze the sequential-state machine shown in the following figure. Obtain state table and state diagram for the same. 
C	Shown below is the state diagram for sequential machine reduce it and design using D Flip Flop.