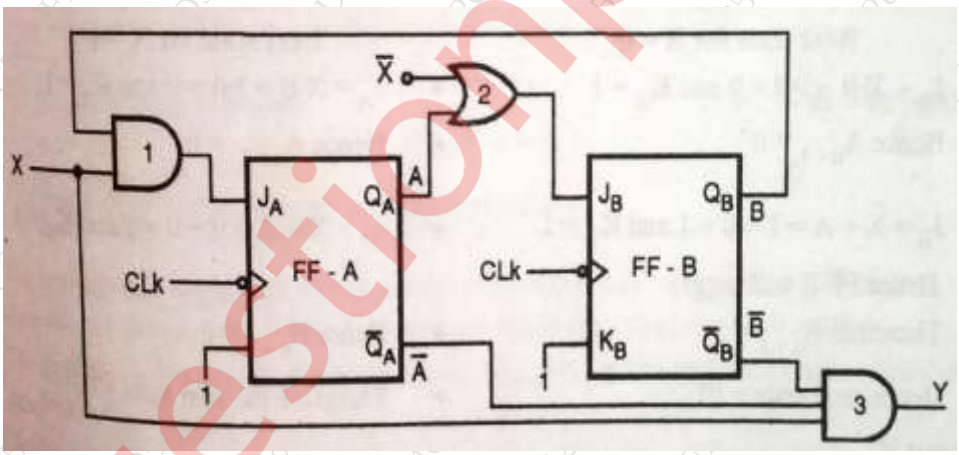
Time: 3 Hrs **Max. Marks: 80**

N.B.: - (1) Question number 1 is compulsory.

(2) Solve any Three from remaining five questions.

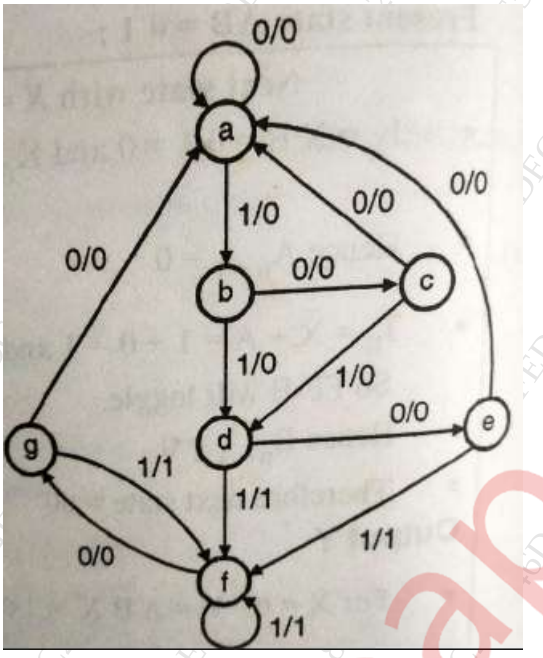
(3) Draw neat logic diagram & assume suitable data whenever necessary.

Q.1	**Solve any four**	**Marks**
a	List any six features of VHDL.	05
b	Differentiate between Mealy and Moore machine.	05
c	Write a VHDL code for Half adder circuit.	05
d	Explain Booth's multiplication with example.	05
e	Write a short note on Register transfer level (RTL).	05
Q.2		
a	Analyze the sequential circuit shown below. Hence derive the state table and state diagram.	10



b	Write a VHDL code for JK flip flop	10
Q.3		
a	Design a Mealy sequence detector circuit to detect an overlapping sequence "1010" using D flip flop and logic gates.	10
b	Write a VHDL code for Traffic light controller system.	10
Q.4		
a	Write a VHDL code for 4 bit UP-DN counter using asynchronous reset.	10

b For a given state diagram obtain a reduced state diagram using state reduction technique. 10



Q.5

a List the features of XC4000 FPGA family and discuss it with the help of neat block diagram. 10

b Write a VHDL code for Booth's multiplier. 10

Q.6 Solve any Four

a Write a short note on different modelling styles used in VHDL. 05

b List the features of complex programmable logic devices. 05

c Write a VHDL code for 2-bit parallel multiplier in data flow modelling. 05

d Write a short note on functional and timing simulation. 05

e Explain VHDL operators with example. 05

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