28|11|2023

Paper / Subject Code: 51323 / Digital Logic Circuits

SE | EIX | Sem-III | CBCGS | R-19 | C-Scheme | DLC | SH-2023

(3 Hours) [Total Marks: 80]

QP-1003916 |

N.B.: (1) Question No. 1 is **Compulsory.**

(2) Attempt **any three** questions out of the remaining **five.**

(3) Each question carries 20 marks and sub-question carry equal marks.

(4) Assume suitable data if required.

1.	(a)	(I) Convert decimal number **0.875** in the binary form. (II) Convert binary number **1010101** in the decimal form. (III) Find two's complement of the number **011101000** (IV) Convert decimal number **346** into octal form. (V) Perform the operation **(57 – 32)** using two's complement method. Use 8-bit representation of numbers.	(5)
	(b)	Implement the functions F1 and F2 using PLA with 3 inputs, 3 product terms, 2 outputs. F1 = ∑m (4, 5, 7), F2 = ∑m (4, 5, 6)	(5)
	(c)	Convert SR Flip Flop to D Flip Flop.	(5)
	(d)	Draw gate level diagram of 1 : 4 De-multiplexer having active low out puts, chip enable and explain its operation.	(5)
2.	(a)	Design a Mod 5 lockout free synchronous up counter using JKMS Flip Flops.	(10)
	(b)	Design 5-bit comparator using only one 4-bit comparator IC 7485 and explain its operation.	(10)
3.	(a)	Write short notes on (I) CPLD architecture (II) Data types in Verilog.	(10)
	(b)	Draw block diagram of synchronous counter IC 74163, explain its operation and Design Mod-13 counter using this IC.	(10)
4.	(a)	Discuss Interfacing CMOS to TTL and TTL to CMOS logic families.	(10)
	(b)	Design a Mealy type overlapping serial sequence detector using D flip flops to detect the sequence 01101.	(10)
5	(a)	Draw TTL two input NAND gate and explain its operation.	(10)
	(b)	Write short notes on (I) De-Morgan Theorems (II) Hamming Code	(10)
6.	(a)	Implement the function using only one 4:1 multiplexer and few gates; Y = F (A, B, C, D) = ∑m (0, 1, 6, 12, 13, 14, 15)	(10)
	(b)	Write a Verilog code for Full Adder using CASE statement.	(10)

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