University of Mumbai

Examinations Summer 2022

Program: **Electronics Engineering**

Curriculum Scheme: Rev2019

Examination: SE Semester III

Course Code: ELC303 and Course Name: Digital Logic Circuits

Time: 2 hour 30 minutes Max. Marks: 80

==========

Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	Convert hexadecimal number ABC into decimal
Option A:	2847
Option B:	2748
Option C:	2478
Option D:	2874
2.	The minimum number of 2-input NAND gates are required to realize a half adder is
Option A:	8
Option B:	5
Option C:	6
Option D:	4
3.	How many IC 74151 required to implement four variable boolean function?
Option A:	4
Option B:	3
Option C:	2
Option D:	1
4.	Which of the following expressions is in the sum-of-products (SOP) form?
Option A:	$(A + B)(C + D)$
Option B:	$(A)B(CD)$
Option C:	$AB(CD)$
Option D:	AB +CD
5.	The characteristics equation for T flip flop is_____
Option A:	Qn* = T Qn' + T' Qn
Option B:	Qn* = T 'Qn' + T Qn
Option C:	Qn* = T Qn' + Qn
Option D:	Qn* = T + T' Qn
6.	An *n*-bit Johnson counter cycles through __ states
Option A:	n
Option B:	2n
Option C:	2^n
Option D:	n^2
7.	In Overlapping Sequence detector
Option A:	the last bit of one sequence does not become the first bit of next sequence
Option B:	the all bits of one sequence become the first bit of next sequence

Option C:	the last bit of one sequence become the first bit of next sequence
Option D:	the first bit of one sequence become the first bit of next sequence
8.	A Mealy machine is a FSM whose
Option A:	output depends on present state
Option B:	output depends on present input as well as present state
Option C:	output depends on present input
Option D:	output depends on only FFs
9.	In a logic family if output logic high is between 3V to 5V and input logic high is 2V to 5V, what is the high level noise margin?
Option A:	0V
Option B:	1V
Option C:	2V
Option D:	3V
10.	For describing circuits like flip flops _____ statement is used
Option A:	entity
Option B:	always
Option C:	component
Option D:	initial

Q.2	**Solve any Four out of Six** **5 marks each** ***Please delete the instruction shown in front of every sub question***
A	Generate 7-bit even parity Hamming code for data 1010
B	Design and implement a Full adder using Half adder.
C	How to overcome race-around condition of JK-FF? Explain in detail.
D	Write a Verilog code for EX-OR gate using Gate-level modelling.
E	Write short notes on Interfacing between CMOS and TTL.
F	Design MOD-10 counter using IC7490

Q.3	**Solve any Two Questions out of Three** **10 marks each**
A	Design Mealy machine to detect overlap sequence 1001
B	Construct 2 input TTL NAND logic gate and explain.
C	Write a Verilog code for Full Adder using CASE statement

Q.4	**Solve**
A	**Solve any Two** **5 marks each**
i.	Convert JK flip flop to T flip flop
ii.	Design a circuit using 2:1 MUX to implement 2-input NAND Gate
iii.	Convert given decimal numbers in Gray code form: 1. $(42)_{10}$ 2. $(17)_{10}$
B	**Solve any One** **10 marks each**
i.	Reduce give logical function using K-map and implement using NAND gates only: $F(A,B,C,D) = \sum m(5,11,13,14,15) + d(4,6,7)$
ii.	Draw a circuit diagram of 4-bit Twisted Ring Counter and also give its output waveforms.