Duration: 3hrs [Max Marks:80]

N.B. : **(1) Question No 1 is Compulsory.**
**(2) Attempt any three questions out of the remaining five.**
**(3) All questions carry equal marks.**
**(4) Assume suitable data, if required and state it clearly.**

1 Attempt any FOUR [20]

a 1-bit 5 stage shift register

b Explain the working of floating gate transistor in Flash memory.

c For enhancement type NMOS transistor threshold voltage $V_T$=0.7V, µnCox =40 µA/V2, W = 30µm, L = 10 µm. Calculate $I_D$ if for VGS = 2 , $V_{DS}$= 2V

d Explain clock distribution in VLSI design.

e Draw HLSM of soda dispenser machine

2 a Consider a CMOS inverter with following parameters: [10]

nMOS VTN = 0.6 V µnCox =60 µA/V2 (W/L)n = 8

pMOS VTp = -0.7 V µpCox =25 µA/V2 (W/L)p = 12

Calculate the $V_{IL}$ and $V_{TH}$. The power supply voltage is VDD = 3.3 V.

b Explain pWell fabrication process with neat diagrams. [10]

3 a Realize SR flip flop using CMOS logic and draw its layout. [10]

b Explain 6T SRAM with its read and write operation. [10]

4 a Realize the expression Y=A(B+C) D using the following logic style. [10]

1. CMOS logic
2. Pseudo NMOS
3. Dynamic Logic
4. Domino Logic

b Implement the following [10]

1. 3x3 Array multiplier
2. 4:1 mux using TG

5 a Implement the following [10]

1. 4 bit carry lookahead adder carry using dynamic logic
2. 8-bit carry bypass adder

b Draw 4 *4 bit NAND based array and NOR based array to store the following data in respective memory locations. [10]

| Memory address | Data |
|---|---|
| 1000 | 0101 |
| 0100 | 1101 |
| 0010 | 0010 |
| 0001 | 1011 |

6 a Design a 'serial FIR filter' using the RTL design process. Draw HLSM,FSM, interface and Datapath [10]

b Realize the expression Y = A+ BC (D+E) +F using CMOS logic. Find equivalent CMOS inverter for simultaneously switching of all input. Assume $(\frac{W}{L})p = 15$, $(\frac{W}{L})n = 10$ [10]

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