1T01033 - S.E.(Electronics and Telecommunication )(SEM-III)(Choice Base Credit Grading System ) (R- 19) (C Scheme) / 51223 - Digital System Design

QP CODE: 10039392 DATE: 28/11/2023

**TIME: 3 Hours** **Maximum Marks: 80**

NB:

1) Question no. 1 is compulsory.
2) Out of remaining questions, attempt any 3 questions.
3) In all 4 questions to be attempted.
4) All questions carry equal marks.
5) Answer to each new question to be started on a fresh page.
6) Figure in brackets on the right hand side indicate full marks for a question.
7) Illustrate answer with neat diagrams wherever necessary.

**Q.1** a) Subtract $(15)_{10}$ from $(25)_{10}$ using two's complement method. **[5]**

b) Explain the basic laws of Boolean Algebra. **[5]**

c) Compare SRAM and DRAM. **[5]**

d) Compare Combinational circuit and Sequential circuit. **[5]**

**Q.2** a) Design a Full Adder and Implement using NAND gates only. **[10]**

b) What is race around condition and explain method to avoid it. **[10]**

**Q.3** a) Minimize the following function using K Map and Implement using NAND Gates. **[10]**

$F(A, B, C, D) = \sum m(0,1,3,7,8,9,11,15)$

b) Develop a mod 6 Synchronous Counter using T F/Fs which counts in the sequence 0-1-2-3-4-5-0. Take care of lockout condition. **[10]**

**Q.4** a) Minimize the following expression using Quine McClusky Technique **[10]**

$F(A, B, C, D) = \sum(0,1,2,3,7,8,9,10,11,13,15)$

b) Convert i) D to T flip flop **[10]**

ii) JK to T flip flop

**Q.5** a) Implement a 4 bit Binary to Gray Code converter using PROM. **[10]**

b) Sketch and explain the working of a 4-bit Asynchronous down counter using JK flip flop. Sketch each output with reference to clock. **[10]**

**Q.6** a) Draw and explain the working of a 4-bit Ring counter with timing diagram. **[10]**

b) Write VHDL program to build a 4:1 Multiplexer. **[10]**

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