Time: 3 Hours **Max. Marks: 80**

Q1 is compulsory. Attempt any three from Q2 to Q6.

Q1 **Solve any Four** **5 marks each**

A Explain the operation of a semiconductor pn junction diode with the help of VI characteristics.

B Explain Miller's capacitance theorem.

C Compare BJT CE amplifier and JFET CS amplifier.

D What is crossover distortion in Class B power amplifiers?

E Let V_{DD} = 5V, $V_{t,1}$ = 1V, $k_{n,1}'$ = 20μA/V^2 and R = 1KΩ. What should be $(W/L)_1$ needed for creating I_{ref} = 1mA? What should be $(W/L)_2$ if I_o = 7mA? Refer Fig. 1

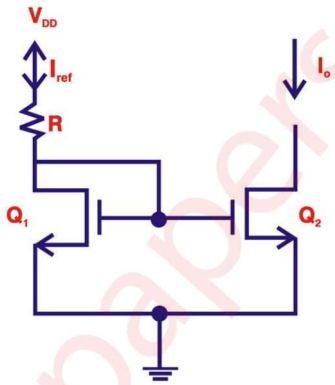

Fig. 1

Q2 **10 marks each**

A Design a feedback bias circuit for n-channel E-MOSFET with operating drain current of 0.5 mA. Given: V_{DD} = 5 V, k'$_n$ = 100 μA/V^2, W = 1.8 μm, L = 180 nm, V_{T0n} = 1 V, Use a standard resistor value for R_D and recalculate I_D and V_D. Refer fig. 2.

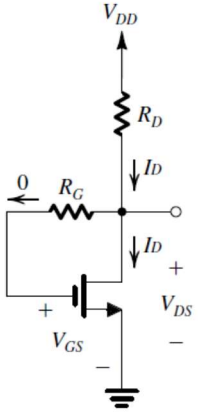

Fig. 2

B Draw a small signal equivalent circuit of an E-MOSFET CS amplifier given in fig. 3 and derive the expression for voltage gain, input resistance and output resistance.

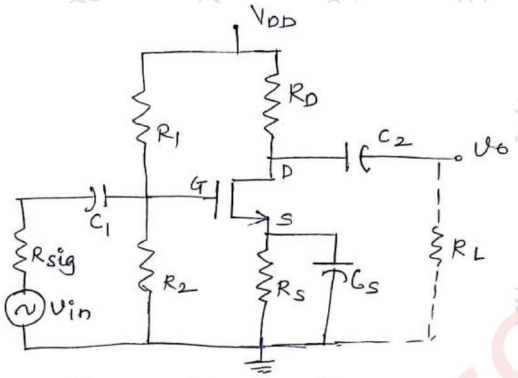

Fig. 3

Q3

A Explain construction and working of n-channel E-MOSFET **5 marks**

B What is thermal runaway and how it can be avoided? **5 marks**

C Calculate low cutoff frequencies due to coupling and bypass capacitors of the circuit given in fig. 4 **10 marks**

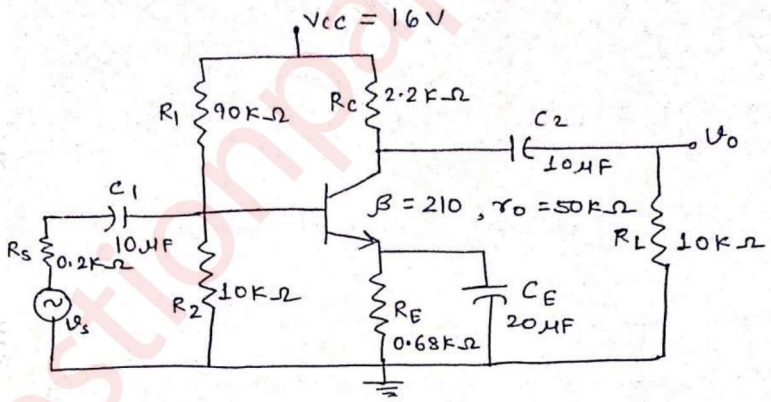

Fig. 4

Q4

A Determine f_β and f_T for the given circuit. Assume I_E = 1.65 mA. Refer Fig. 5 **5 marks**

$R_s = 1\,\text{k}\Omega, R_1 = 40\,\text{k}\Omega, R_2 = 10\,\text{k}\Omega, R_E = 2\,\text{k}\Omega, R_C = 4\,\text{k}\Omega, R_L = 2.2\,\text{k}\Omega$

$C_s = 10\,\mu\text{F}, C_C = 1\,\mu\text{F}, C_E = 20\,\mu\text{F}$

$h_{fe} = 100, r_o = \infty\ \Omega, V_{CC} = 20\ \text{V}$

$C_\pi(C_{be}) = 36\,\text{pF}, C_u(C_{bc}) = 4\,\text{pF}, C_{ce} = 1\,\text{pF}, C_{W_i} = 6\,\text{pF}, C_{W_o} = 8\,\text{pF}$

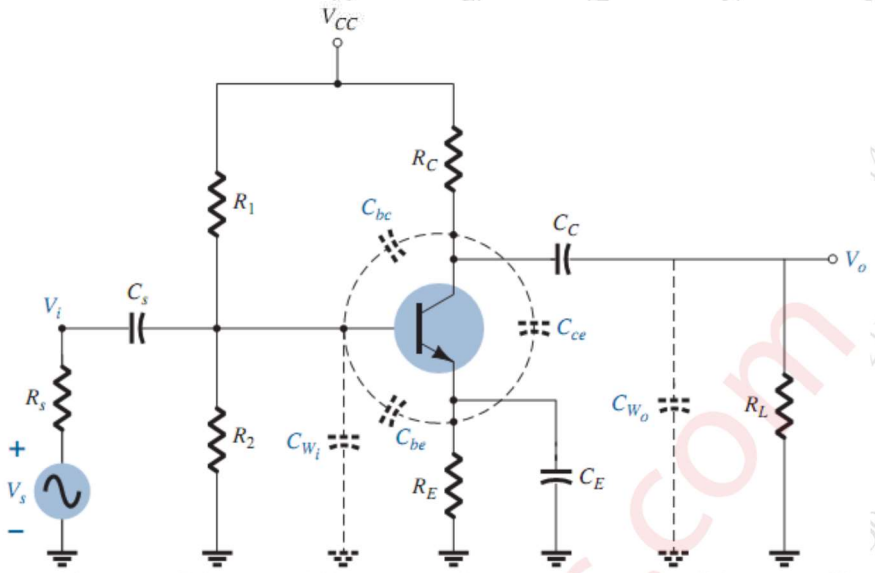

Fig. 5

B Draw and explain high frequency model for BJT in CE configuration. **5 marks**

C Draw and explain a series fed class A power amplifier with the help of neat diagram and waveforms and derive the expression of power efficiency. **10 Marks**

Q5

A Design a voltage divider bias circuit to operate at the given conditions. Calculate the stability factors S(ICO), S(VBE), S(β). Refer Fig. 6 **10 Marks**

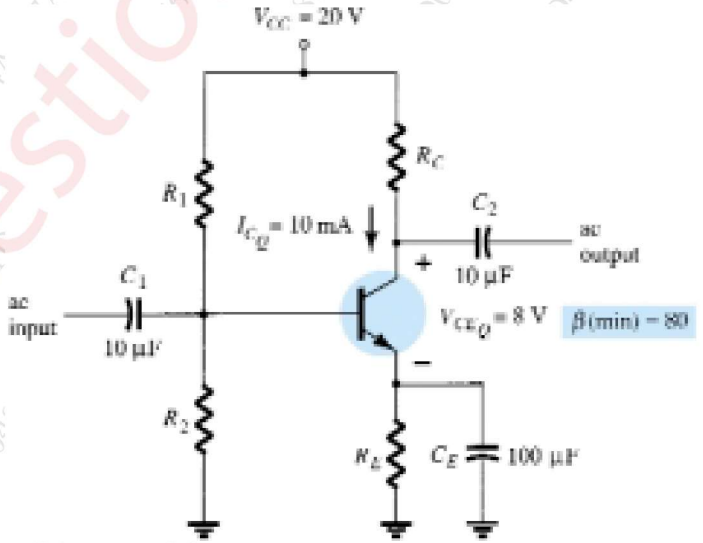

Fig. 6

B Determine the input impedance, output impedance, voltage gain and current gain for the given circuit. Refer fig. 7 **10 Marks**

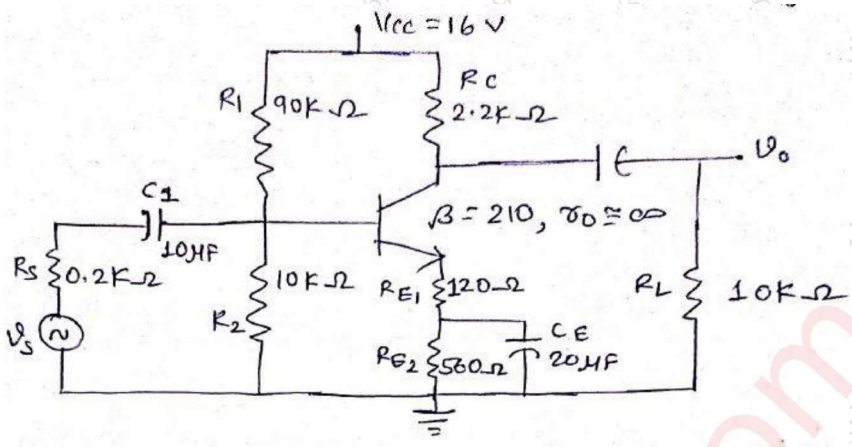

Fig. 7

Q6

A Derive the equation of CMRR for the MOS differential pair amplifier. **10 Marks**

B Write short note on:

i) E-MOSFET as a differential amplifier **5 Marks**

ii) Zener diode as a voltage regulator **5 Marks**