SEC SEM-III) / COMP / R-19 / FH-22 / DLCA / 13.06.22 (E)

Q.P CODE: 94821

University of Mumbai

Examinations Commencing from

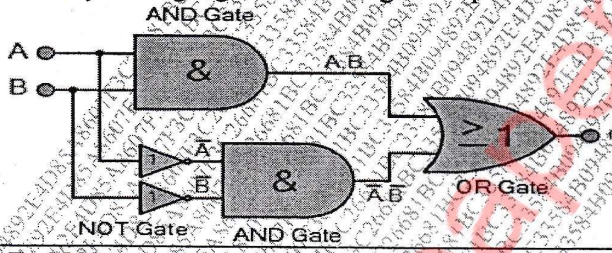
Program: Bachelor of Engineering in Computer Engineering

Curriculum Scheme: Rev2019

Examination: DSE Semester III

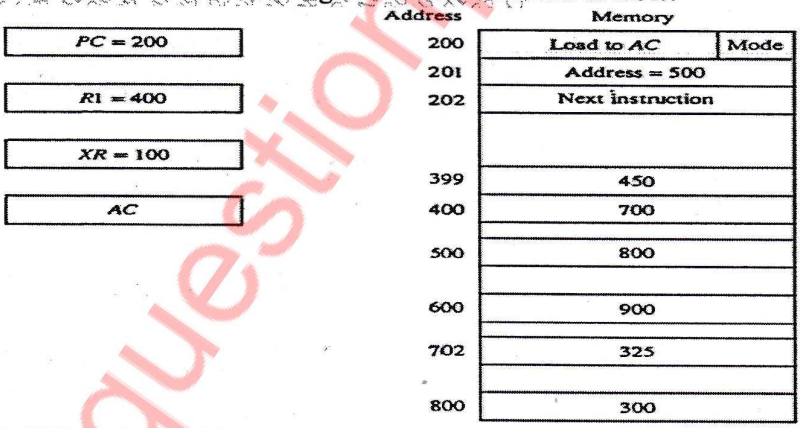
Course Code: **CSC304** and Course Name: **Digital Logic & Computer Architecture**

Time: 2 hour Max. Marks: 80

Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks. (2 marks each, total 20 marks)**
1.	Let, $x_1 \oplus x_2 \oplus x_3 \oplus x_4 = 0$, where x_1, x_2, x_3, x_4 are Boolean variables, and $\oplus$ is the XOR Operator. Which one of the following must always is True?
Option A:	$x_1 x_2 x_3 x_4 = 0$
Option B:	$x_1 x_3 + x_2 = 0$
Option C:	$\overline{x_1} \oplus \overline{x_3} = \overline{x_2} \oplus \overline{x_4}$
Option D:	$x_1 + x_2 + x_3 + x_4 = 0$
2.	Identify the logic gate based on given equivalent circuit. 
Option A:	Ex-NOR gate
Option B:	Ex-OR gate
Option C:	NAND gate
Option D:	NOR gate
3.	The addition of −37 and +18 integer numbers using the 2's complement method, is
Option A:	$(11101101)_2$
Option B:	$(10101101)_2$
Option C:	$(11111101)_2$
Option D:	$(11100101)_2$
4.	Following microinstruction sequence is denote which cycle in the instructional cycle. PC_{out}, MAR_{in}, Read, Slect4, Add, Z_{in} Z_{out}, PC_{in}, Y_{in}, WMFC MDR_{out}, IR_{in}
Option A:	Instruction fetch
Option B:	Instruction decode
Option C:	Address calculation of Operand
Option D:	Instruction execution
5.	SDRAM stands for _____ and DDR stands for _____

Option A:	Synchronous dynamic Random-Access Memory, Double Data rate
Option B:	Synchronous dynamic Read/Write Access Memory, Double Data rate
Option C:	Static Dynamic Random-Access Memory, Dynamic Data rate
Option D:	Static Dynamic Random-Access Memory, Double Data rate
6.	Suppose that a bus has 16 data lines and requires 4 cycles of 250 nsecs each to transfer data. The bandwidth of this bus would be 2 megabytes/sec. If the cycle time of the bus was reduced to 125 n secs and the number of cycles required for transfer stayed the same. What would the bandwidth of the bus?
Option A:	1 Megabyte/sec
Option B:	2 Megabytes/sec
Option C:	4 Megabytes/sec
Option D:	8 Megabytes/sec
7.	Which of the following statement is false with respect to instruction pipeline?
Option A:	Pipelining can increase the throughput of a system.
Option B:	Pipelining partitions the system into multiple independent stages with added buffers between the stages.
Option C:	Pipelining reduce the latency of each individual instruction.
Option D:	Unbalanced lengths of pipeline stages reduces overall speedup.
8.	Select true statement from the following.
Option A:	USB is a parallel mode of transmission of data and this enables for the fast speeds of data transfers.
Option B:	In USB the devices can communicate with each other.
Option C:	The type/s of packets sent by the USB is/are Data.
Option D:	When the USB is connected to a system, its root hub is connected to the Processor BUS.
9.	32-bit PCI expansion slots on a motherboard provides speed
Option A:	Half-duplex: 33 MB/s (32-bit at 33 MHz – the standard configuration) 266 MB/s (32-bit at 66 MHz) 66 MB/s (64-bit at 33 MHz) 33 MB/s (64-bit at 66 MHz)
Option B:	Half-duplex: 133 MB/s (32-bit at 33 MHz – the standard configuration) 266 MB/s (32-bit at 66 MHz) 266 MB/s (64-bit at 33 MHz) 533 MB/s (64-bit at 66 MHz)
Option C:	Half-duplex: 166 MB/s (32-bit at 33 MHz – the standard configuration) 266 MB/s (32-bit at 66 MHz) 266 MB/s (64-bit at 33 MHz) 566 MB/s (64-bit at 66 MHz)
Option D:	Half-duplex: 128 MB/s (32-bit at 33 MHz – the standard configuration) 266 MB/s (32-bit at 66 MHz) 266 MB/s (64-bit at 33 MHz) 566 MB/s (64-bit at 66 MHz)
10.	In three-address instruction, the program to evaluate X = (A + B) • (C + D) is ADD R1, A, B // R1 → M[A] + M[B] // // M[X] symbolizes the memory word located at address X.// …… MUL X, R1, R1 // M[X] ← R1 * R2 // Missing 2nd statement is ….
Option A:	ADD R1, C, D // R1 → M[C] + M[D] //
Option B:	ADD R2, C, D // R2 → M[C] + M[D] //
Option C:	ADD R3, C, D // R3 → M[C] + M[D] //
Option D:	ADD R4, C, D // R4 → M[C] + M[D] //

Q.2	Solve any Four out of Six.	
A)	Compare the terms Computer organization with Computer architecture.	05
B)	Perform the following – i) Convert $(340)_{10}$ to excess-3 code. (1 mark) ii) Convert Hexadecimal to decimal: DADA (2 marks) iii) Hexadecimal to binary conversion: 3A9D.A0C (2 marks)	05
C)	Design a full adder using half adder and additional gates. Give its truth table.	05
D)	Give the advantages and disadvantages of hardwired control unit design using state-table method and Delay-element method.	05
E)	What is Cache Memory? A 32-bit computer has a 32 bit memory address. It has 8kB of cache memory. The computer follows four-way set associative mapping. Each line size is 16 bytes. Show the memory address format and cache memory organization.	05
F)	What is Amdahl's Law? Let a program have 40 percent of its code enhanced (so $f_E = 0.4$) to run 2.3 times faster (so $f_I = 2.3$). What is the overall system speedup S?	05
Q.3	**Solve any Four out of Six.**	
A)	Multiply $(10)_{10}$ with $(8)_{10}$ using booths multiplication algorithm.	05
B)	Convert 39887.5625 to IEEE 64-bit Double precision floating point format.	05
C)	Following diagram represents the addressing modes of processor. Considering given numerical values calculate the effective address and content of AC register value for different addressing modes as mentioned in table.	05



Sr. no.	Addressing Mode	Effective address	Content of AC
1	Direct address		
2	Immediate Operand		
3	Relative address		
4	Indexed address		
5	Register indirect		

	D)	Write microprogram for instruction MOV A, B (copy the contents of Register B to Register A).	05
	E)	Explain with suitable diagrams, why DRAM cell required refreshing in Computer System?	05
	F)	Draw the neat block diagram for Flynn's classification.	05
Q.4	**Solve any Four out of Six.**		
	A)	Draw basic organization of computer and explain its block level functional units.	05
	B)	Using step by step restore division algorithmic procedure solve the following: 11 (Dividend) / 3 (Divisor).	05
	C)	Draw logic circuit diagram Master-Slave J-K flip-flop with PRESET and CLEAR inputs using NAND gates. Give its truth table and logic symbol diagram.	05
	D)	Draw and explain functioning of the microprogrammed control unit.	05
	E)	Write a short note: Interleaved and Associative memory.	05
	F)	Enlist different types of bus arbitration schemes and explain any one.	05