INST CBGS

TE|V|INST| Signal Conditioning Ckt Design / 01·12·15

Q.P. Code : 5653

(3 Hours) **[Total Marks : 80**

Note : 1. Question no. 1 is **compulsory**

2. Attempt any **three** questions from remaining **five** questions

3. Figures to the right indicate full marks

4. Assume suitable data whenever necessary

Duration : 03 hours Marks : 80

Q.1. a. With a suitable diagram discuss the concept of loading and how to avoid it. 20

b. Draw the circuit of practical Integrator and its output waveforms.

c. Draw the circuit of Zero crossing detector and its output waveforms.

d. Explain the significance of all-pass filters.

Q.2. a. Explain successive approximation analog to digital converter with diagram.10

b. Draw and explain circuit diagram of absolute value circuit using op-amp. Discuss its advantages over traditional diode rectifier. 10

Q.3. a. Draw and explain the operation of Temperature compensated Log amplifier. 10

b. What are the advantages of active filters over passive filters. Design a second-order band pass filter for given F_H=2KHz, F_L=300Hz and Pass band gain=4. 10

Q.4. a. Design and Explain operation of Astable Multivibrator using IC555 for 60% duty cycle. 10

b. A sensor outputs a range of 20.0 to 250mVas a variable varies over its range. Develop signal conditioning so that this becomes 0 to 5V. The circuit must have very high input impedance. 10

Q. 5. A RTD has α[]=0.005/°C, R=500Ω, and a dissipation constant of PD=30mW/°C at 20°C. The RTD is used in a bridge circuit with $R_1 = R_2 = 500\Omega$ and R_3 a variable resistor used to null the bridge. If the supply is 10 V and the RTD is placed in a bath at 0°C, find the value of R_3 to null the bridge. 10

b. Draw and explain the principle and construction of thermocouple. What is the signal conditioning associated with it. 10

Q.6: Write short notes on : (**any four**) 20

a. Sample and hold circuit

b. Phase Locked loop

c. Variable voltage regulator

d. Data Acquisition System

e. Flash type ADC

f. SMPS