

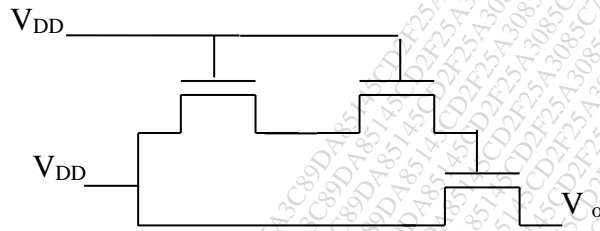
Time: 3 Hours

Marks: 80

- 1] Question no.1 is compulsory
- 2] Attempt any three questions out of remaining questions
- 3] Assume suitable data if required
- 4] Figures to the right indicate marks.

Q. No. 1) Solve the following [20]

- a) Calculate the voltage at the output node V_o if $V_{DD}=5V$ and $V_{th}=1.5V$



- b) Draw and Explain Clocked SR latch using static CMOS design style.
- c) Draw layout diagram of static CMOS inverter based on lambda design rules.
- d) Draw VTC of static CMOS inverter and show operating regions of nMOS and pMOS transistors on it.
- e) Explain short channel effects (any two).

Q. No. 2)

- a) Explain in detail the fabrication process steps for a CMOS inverter using n- well process with the help of cross sectional view for each step. [10]
- b) Implement a two input XOR gate using
 - (i) static CMOS logic
 - (ii) Dynamic logic
 - (iii) Transmission gate
 - (iv) Pseudo NMOS logic
 [10]

Q. No. 3)

- a) Derive an expression for the inverter threshold voltage (switching voltage) of a CMOS inverter. Calculate the (W/L) ratios of the NMOS and PMOS transistor in the CMOS inverter circuit with the following parameters:

$$V_{DD} = 3V \quad V_{t0,n} = 0.6V \quad V_{t0,p} = -0.8V \quad V_{TH} = 1.5V$$

$$\mu_n C_{OX} = 60 \mu A/V^2 \quad \mu_p C_{OX} = 20 \mu A/V^2 \quad [10]$$

- b) Draw schematic diagram of six transistor SRAM cell and explain its Read and Write operations. [10]

Q. No. 4)

- a) What is scaling. Compare constant field scaling with constant voltage scaling and state advantages and limitations in both the methods. [10]
- b) Design a 4- bit CLA adder using dynamic NMOS logic. Compare delay of this circuit with respect to a 4 bit ripple carry adder. [10]

Q. No. 5)

- a) Draw the CMOS circuit for $Y = \overline{A + BC(D + E) + F}$ and find an equivalent CMOS inverter circuit for simultaneous switching of all inputs, assuming that $(W/L) = 15$ for all pMOS transistors and $(W/L) = 10$ for all nMOS transistors. [10]
- b) Explain in detail static and dynamic power dissipation. What are the main components which make power dissipation in CMOS circuit? [10]

Q. No.6) Explain any 2 of the following [20]

- a. 4 bit Array Multiplier
- b. Interconnect Delay model
- c. 3-T DRAM