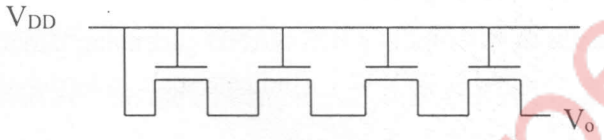
Q. P .Code: 36647

Duration: 3 Hours **Marks:80**

1] Question no.**1** is **compulsory**
2] Attempt any **three** questions out of remaining questions
3] Assume **suitable data** if **required**

Q. No. 1) Attempt any four from the following [20]

a) Calculate the voltage at the output node V_o if V_{DD}=5V and V_{th}=1.5V



b) Implement 2:1 multiplexer circuit using pass transistor logic and state its drawback. Draw the circuit using CMOS transmission gates.

c) State the conditions required for the symmetric static CMOS inverter.

d) Compare ion implantation with diffusion stating its advantages and disadvantages.

e) In 2-input CMOS NAND gate all PMOS transistors have (W/L)p = 20 and all NMOS transistors have (W/L)n = 10. Draw its equivalent CMOS inverter for simultaneous switching of all inputs and find size of PMOS and NMOS transistor in the equivalent inverter circuit.

Q. No. 2)

a) A CMOS inverter has following parameters
V_{DD} = 3.3V $V_{t0,n}$= 0.6V $V_{t0,p}$ = -0.7V
K_n =200μA/V^2 Kp =80μA/V^2
Calculate the noise margin of the circuit. Is the inverter symmetric? [10]

b) Implement $Y= \overline{A(B+C) +DE}$ [10]
(i) static CMOS logic
(ii) Dynamic logic
(iii) Depletion load logic
(iv) Pseudo NMOS logic

Q. No. 3)

a) Explain in detail the fabrication sequence of PMOS transistor with cross sectional view of each step. [10]

b) Draw schematic and layout diagram of six transistor SRAM cell and explain Read and write operations. [10]

Q. No. 4)

a) Compare constant field scaling with constant voltage scaling and state advantages and limitations in both the methods. Show the effect of scaling on power density and current density. [10]

b) Design a 3- bit carry generator block of carry look ahead adder using multiple output domino logic (MODL) style. Explain how it achieves better speed compared to ripple carry adder. [10]

Q. No. 5)

a) Draw layout diagram of two input CMOS NAND gate using lambda design Rules with $(L/W)_P=1/2$ and $(L/W)_n=2/1$. (Indicate scale in terms of lambda on layout). [10]

b) Draw transistor level CMOS negative edge triggered master slave D flip flop. [5]

c) What are the limitations of single phase clock? Explain with neat diagram two phase clock system. [5]

Q. No. 6) Write short notes on any four [20]

i) ESD protection circuit.
ii) 4x4 Barrel shifter
iii) MOSFET Capacitances
iv) Design rules and their necessity
v) Clock skew and clock jitter

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