Q.P.Code:16055

Time: 3 Hours **Marks: 80**

Please check whether you have got the right question paper.

N.B. : 1. Question No. ONE is compulsory
2. Solve any THREE out of remaining questions
3. Assume suitable data if required

Q1. Solve the following **20 Marks**

A. Show the current drawn by CMOS inverter on VTC and justify that CMOS inverter draws maximum current during switching.

B. Compare all types of MOSFET based inverters. Clearly draw their circuits and also mention their advantages and limitation/drawbacks.

C. Two lines on an interconnect level are separated a spacing of S=0.60 μm. Each individual line has w=0.30 μm, T_{ox}=1.0 μm and t=1 μm. Calculate the coupling capacitance per unit length C_C. Also find the coupling capacitance if the interaction length is 25 μm.

D. In short, explain what is pass transistor logic? With suitable example explain when you will prefer pass transistor logic and when transmission gate.

Q2. A. Calculate τfall using average current method for CMOS inverter with following parameters: **05 Marks**

Power supply voltage V_{DD}=3.2 V
Output load capacitance = 0.1 pF
$\mu_n C_{ox}$=20 μA/V2
$(W/L)_n$=20
$V_{T,n}$=1.0 V

B. For the function $Z = \overline{(A+B)(E+F)(H+I)}$ **05 Marks**

(i) Domino CMOS circuit
(ii) Draw an equivalent circuit for domino circuit by using equivalent transistor sizes with W/L=30/2 (both for NMOS and PMOS)

C. Design CMOS inverter such that the switching threshold is V_{th} = 1.2 V, with the following device parameters:

NMOS: $V_{T0,n}$= 0.6 V $\mu_n C_{ox}$=60 μA/V^2
PMOS: $V_{T0,p}$= −0.8 V $\mu_p C_{ox}$=20 μA/V^2
Assume V_{DD}= 2.4 V and λ=0 **10 Marks**

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Q3. A. Design the circuit and draw layout for the function $Y = \overline{(D + E + F)(B + C + A)}$ using CMOS logic. Also find equivalent CMOS inverter circuit for simultaneous switching of all inputs assuming that $(W/L)_P$=30 for all PMOS transistors and $(W/L)_n$=10 for all NMOS transistors. **10 Marks**

B. What are the problems of Domino logic? Also suggest remedy for these problems. **10 Marks**

Q4. A. With neat diagrams explain the read and write operation of 3T DRAM cell. **10 Marks**

B. Explain in detail design strategy of 6T SRAM Cell. Also draw the layout for 6T SRAM cell. **06 Marks**

C. Draw MOSFET based Master Slave JK Flip Flop **04 Marks**

Q5. A. Construct the complementary static CMOS full adder. Now propose another full adder which will take less number of transistors as compared to complementary static CMOS full adder. **10 Marks**

B. Draw and explain 4 X 4 multiplier array. **06 Marks**

C. Justify that even if LEVEL 1 MOSFET model already exists there is necessity of LEVEL 2 MOSFET Model. **04 Marks**

Q6. A. With suitable diagrams explain clock stabilization in VLSI Chip. **05 Marks**

B. What is the need of input and output ports in CMOS circuits? Explain with neat schematic bidirectional IO port. **05 Marks**

C. Explain different components of leakage power in CMOS **05 Marks**

D. Explain DIBL and velocity saturation in short channel device. **05 Marks**
