TE- SEM VI (CBGS) - EXTC 7/6/2016

VLSI Design

**Q.P. Code : 588801**

**(3 Hours)** **[Total Marks : 80**

**N.B. :** (1) Question **ONE** is **compulsory**.
(2) Solve **any THREE** out of remaining **questions**.
(3) Draw **neat** and **clean diagrams**.
(4) Assume **suitable data** if **required**.

1. Attempt **any FOUR** from the following : **20**
   (a) For NMOS resistive load inverter with $R_L$ = 50K find $V_{IL}$ and $V_{OL}$ if $V_{DD} = 5V$, $V_{TO} = 1\,V$, $K_n = 100\ \mu A/V^2$, neglect body bias effect and channel length modulation.
   (b) With help of appropriate circuit diagram and waveforms, explain charge sharing problem of dynamic logic. How to overcome the same.
   (c) Explain the significance of Level - 1 MOSFET model parameters.
   (d) Implement 4: 1 MUX using Transmission gate technology.
   (e) Explain advantages and disadvantages of Pass Transistor logic in VLSI Design.

2. (a) Explain working of CMOS Inverter with help of Voltage Transfer Characteristics and derive expression for $V_{IL}$ and $V_{IH}$. **10**
   (b) Implement 1 - bit full adder circuit using standard CMOS logic, dynamic logic and pseudo NMOS logic. **10**

3. (a) Draw six transistors SRAM cell and explain its read 0, read 1, write 0 and write 1 operation with the help of appropriate waveforms. **10**
   (b) What is Carry Look Ahead (CLA) adder. Write equations for carry bits of 5-bit CLA in terms of input bits only i.e carry generate and carry propagate and implement the same using domino logic. **10**

4. (a) For 2 input CMOS NAND gate find $V_{OL}$, $V_{OH}$, $V_{IH}$, and $V_{IL}$. Assume that both the inputs are switching simultaneously. Consider NMOS and PMOS with following parameters. $V_{DD} = 5V$, $V_{TOn} = 1\,V$, $K_n = 100\mu A/V^2$, $V_{TOp} = -1V$, $K_p = 25\mu A/V^2$. **10**
   (b) Give NMOS fabrication process flow with help of neat sketches of appropriate masks and cross section at each process steps. **10**

**TURN OVER**

5. (a) Implement 4x4 NAND based ROM array to store "1001", "0101", "1010" and "1100" in the memory. **5**

   (b) Explain the effect of Interconnect scaling on various performance parameters of VLSI circuits. **10**

   (c) Draw layout of 3 transistor (3-T) DRAM cell using lambda rules. **5**

6. Write short notes on **any FOUR** : **20**

   (a) Power Distribution schemes

   (b) Array Multiplier

   (c) Interconnect Delay Model

   (d) NAND Flash Memory

   (e) Column Decoders

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