Paper / Subject Code: 88945 / Elective - II Digital VLSI Design

16-Dec-2019   02:30 pm - 05:30 pm   1T01026 - T.E.(Electronic & Telecommunication Engineering)(SEM-VI)
(Choice Base) / 88945 - Elective - II Digital VLSI Design 79920

(**3 Hours**)   (**Total Marks : 80**)

Please check whether you have got the right question paper.

N.B.:   1)   **Question No.1** is **compulsory**.

2)   Solve **any three** from remaining **five** questions.

1.	a)	Explain charge sharing in brief.	**(04)**
	b)	Write a program for 3:8 decoder in HDL.	**(04)**
	c)	Explain different Clock generation styles in brief.	**(04)**
	d)	Compare Semi custom and full custom design.	**(04)**
	e)	Draw HLSM for Soda dispenser machine.	**(04)**

2.   a)   Explain I-bit adder and Implement sum and carry circuit using CMOS.   **(10)**

   b)   Implement the following using different MOS design styles :   **(10)**

   1)   XNOR gate using Static CMOS,

   2)   Y = not (A + BC) using Dynamic CMOS,

   3)   Y = (A + BC + DE + F) using Pseudo NMOS and

   4)   XOR gate using Domino logic style.

3.   a)   Draw and explain operation of 6-T SRAM in detail.   **(10)**

   b)   Design Sum of absolute differences circuit using RTL design technique. Draw   **(10)**
HLSM, Data path, Interface and Controller FSM.

4.   a)   Realize D-Latch using Tristate and DFF using TG gate and write a program for   **(10)**
DFF in HDL.

   b)   Design 4X4 array multiplier.   **(05)**

   c)   Implement Barrel shifter circuit using MOS.   **(05)**

5.   a)   Implement SR latch using CMOS design and draw its layout using λ based rules.   **(10)**

   b)   Explain Carry select Adder circuit in detail.   **(05)**

   c)   Design HLSM for laser based distance measure.   **(05)**

6.   Write short notes on :

   a)   Input circuit.   **(05)**

   b)   Flash memory.   **(05)**

   c)   Interconnect Delay Model.   **(05)**

   d)   ROM.   **(05)**

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