

3 Hours

[Total Marks 80]

NB: 1. Question No. 1 is compulsory

2. Solve any three questions from remaining

3. Assume suitable data whenever necessary and justify the assumption.

- Q.1. a) I is possible to realize the logic function $F(A, B, C) = \sum m(1, 2, 4, 7)$ using a single threshold gate? 05
- b) What is incompletely specified machines and how to specify using compatible states? 05
- c) Differentiate between Mealy and Moor type state machine. 05
- d) Differentiate between Synchronous and Asynchronous sequential circuits. 05
- Q.2. a) Draw the state diagram and the state table for Moore type sequence detector to detect the sequence 101. 10
- b) Using Quine-McCluskey method of tabular reduction minimize the given combinational single output function $f(W, X, Y, Z) = \sum m(0, 1, 5, 7, 8, 10, 14, 15)$ 10
- Q.3. a) Realize the Boolean function using threshold gate $F(x_1, x_2, x_3, x_4) = \sum m(0, 1, 4, 5, 8, 9, 11, 13)$ 10
- b) Obtain the minimal SOP and POS expression for the following: 10
- $$f = \sum m(0, 2, 7, 8, 10, 13, 16, 18, 24, 26, 29, 31, 32, 34, 37, 39, 40, 42, 45, 47, 48, 50, 53, 55, 56, 58, 61, 63)$$
- Q.4. a) What are the components of ASM chart? Draw an ASM chart to describe a mealy state machine that detects a sequence of 101 and that asserts a logical 1 at the output during the last state of the sequence. 10
- b) Design a 3-bit counter which counts in the following sequence using T flip flop.
 $0 \rightarrow 1 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 7 \rightarrow 0 \dots \dots \dots \text{etc.}$
- Q.5. a) Explain homing and synchronizing sequence techniques with example. 10
- b) i) Explain the state equivalence & distinguishable state in Finite state machine. Reduce the state machine M by partition method. 10

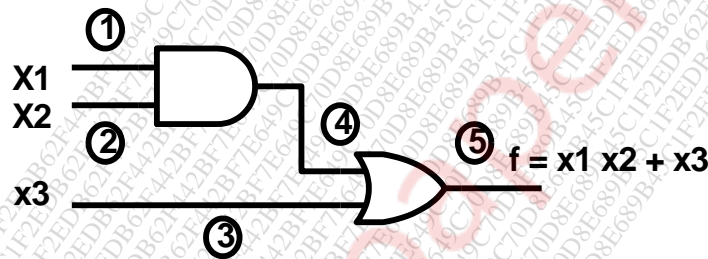
Table No. 1

PS	NS		z	
	x=0	x=1	x=0	x=1
A	E	C	0	0
B	F	C	0	1
C	E	A	0	0
D	F	A	0	1
E	A	D	0	0
F	D	E	0	1

ii) Write a state equations for the reduces machine M in above question and realized it using gates.

- Q.6 a) i) Find the fault table for all stuck-at faults of the following circuit
 ii) prepare test generation using exclusive or method

10



- b) The set {a,b,c,d,e,f,g,h,i,j,k} has the partitions

10

$$\pi_1 = \{a, b, c; d, e, f; g, h, i, j, k\}$$

$$\pi_2 = \{a, b; c, g, h; d, e, f; i, j, k\}$$

$$\pi_3 = \{a, b, c, f; d, e, g, h, i, j, k\}$$

- i) Find $\pi_1 + \pi_2$ and $\pi_1 \cdot \pi_2$
- ii) Find $\pi_1 + \pi_3$ and $\pi_1 \cdot \pi_3$
- iii) Find a partition that is greater than π_1 and smaller than π_3 .
