(3 Hours) [Total Marks: 80]

N.B.: (1) Question No. 1 is **Compulsory**.

(2) Attempt any **three** questions out of **remaining five**.

(3) Assume suitable data if required.

1.		Solve any 4 of the following;	(20)
	(a)	What are the timing issues in synchronous circuit design?	(5)
	(b)	Implement $Z = \overline{(A+B+C)}$ D.E using CMOS gate.	(5)
	(c)	What is the difference between a pass transistor logic and transmission gate?	(5)
	(d)	Compare BJT and CMOS technology in VLSI design.	(5)
	(e)	How speed is improved in carry look ahead adder?	(5)
2.	(a)	Explain noise margin of an nMOS inverter using VTC, critical voltages and input-output window profile.	(10)
	(b)	Compare SRAM and DRAM. Draw write and read circuitry of SRAM and explain its operation.	(10)
3.	(a)	Implement 4*4 barrel shifter using transmission gate and explain in brief.	(10)
	(b)	Explain various clock skews and describe techniques to minimize it.	(10)
4.	(a)	Explain CMOS inverter characteristics mentioning its all regions of operation. What is the effect of changing W/L ratio on it? Explain with example.	(10)
	(b)	Explain various ESD protection techniques.	(10)
5	(a)	Implement 4:1 MUX using pass transmission logic. Explain advantages of using transmission gates.	(10)
	(b)	Draw 1T DRAM cell and explain its write, refresh and read operation.	(10)
6.		Write short notes on any Three of the following:	(20)
	(a)	Switching characteristics of CMOS inverter.	
	(b)	Short channel effects	
	(c)	Importance of low power design.	
	(d)	ESD and its protection.	

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