T.E Sem VI (CBGS)
(ETRX)

DSP.

Q.P. Code : 592001

(3 Hours)   [Total Marks : 80

N.B. : (1) Question number **1** is **Compulsory**.
        (2) Solve any **three** question out of remaining
        (3) Assume suitable data if required.

1. Answer any **four**
    (a) Differntiate between Butterworth and chebyshev filter   5
    (b) Explain the concept of pipelining in DSP processor   5
    (c) Expalin frequency warping effect in designing IIR filter using BLT 5
         method.
    (d) Explain Quantization effect in computation of DFT   5
    (e) State the relationship between DFS, DFT and z Transform   5

2. (a) Compute IDFT of the following sequence using inverse FFT algorithm. 10
         $x(k) = \{3,0,3,0,3,0,3,0\}$
    (b) Prove the Parseval's theorem for the sequence $x(n) = \{2,4,2,4\}$ 5
    (c) Find the linear convolution and circular convolution of the sequences 5
         $x(n) = \{1,2,1,2\}$ and $h(n) = \{4,0,4,0\}$

3. (a) Design an analog Butterworth filter that has - 2dB passband attenuation 10
         at frequency of 20 rad/sec and atleast -10dB stopband attenuation at
         30 rad/sec.
    (b) Convert the following filters with system functions   10

         (i) $H(s) = \dfrac{1}{(s+2)(s+0.6)}$

         (ii) $H(s) = \dfrac{(s+0.1)}{(s+0.1)^2 + 9}$

         into a digital filter by means of impulse invariant and BLT method.

4. (a) Explain the concept of linear phase in FIR filter.   10
         prove the following statement 'a filter is said to have linear phase
         response if its phase response is $\theta(w) = -\alpha w$.
    (b) Design a low pass FIR filter with 7 coefficients for the following 10
         specifications passband frequency = 0.25 khz and sampling frequency
         = 1 khz. Use hamming window in designing.

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5. (a) Draw neat architecture of TMS 320C67xx DSP processor and explain each block. **10**

   (b) Explain addressing modes of DSP processor with example. **10**

6. Write short notes on:- (any **three**) **20**
   - (a) Subband coding
   - (b) Application of DSP processor to Radar signal processing
   - (c) Limit cycle oscillations
   - (d) Product quantization error and input quantization error

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