Sem-VI (CBGS) ETRX 20/5/16.

Computer Organization

Q.P. Code : 591801

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question **No.1** is **compulsory**.
(2) Attempt **any Three** questions from remaining **questions**.
(3) **All** questions carry **equal marks**.
(4) **Figures** to the **right** indicate **full marks**.

1. (a) Explain single and double precision format for floating point number representation. **5**
(b) Write in brief on nano-programming. **5**
(c) Draw Register structure of IA-32 family. **5**
(d) Explain SIMD computer organization. **5**

2. (a) Explain performance measure of computer architecture and factors to improve the performance of the system. **10**
(b) What is microprogramming ? Draw and explain Micro programmed control unit. **10**

3. (a) Explain sequence counter method of implementing Hardware control unit. **10**
(b) What is LRU Algorithm? Find the page fault for the following string using FIFO and LRU page replacement policies for the page address stream 6 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 5. Consider page frame size n = 3. **10**

4. (a) What are the different cache mapping techniques? **10**
Consider a cache consisting of 128 blocks of 16 words each, for a total of 2048 (2k) words and assume that the main memory is addressable by a 16 bit address and it consists of 4k blocks. How many bits are there in each of the TAG, BLOCK/SET and WORD fields for different mapping techniques.
(b) Explain in brief about various DMA transfer modes. **10**

5. (a) Explain Address translation with respect to virtual memory. Hence explain use of Translation Look aside Buffer (TLB). **10**
(b) Compare RISC and CISC architectures. **5**
(c) Write a note on addressing modes of IA- 32 family. **5**

6. (a) Explain data hazard and code hazard in pipelining. Mention solutions to minimize the hazards. **10**
(b) What is bus contention? How is it resolved by using bus arbitration? Explain various bus arbitration methods. **10**
