TE, Sem.-VI, Electronics, FH2018 14/05/18

Ref VI-Elec Basics VLSI D.

Q. P. Code: 37282

[Time: 3 Hours] **[Marks:80]**

Please check whether you have got the right question paper.

N.B:
1. **Question 1 is compulsory**
2. **Solve any tree out of reaming.**
3. **Assume suitable data if necessary**
4. **Draw proper diagrams**

Q.1 Solve any four. 20

a. What are different MOS capacitances? Explain in brief.

b. Implement $Y=\overline{(A+B).(C+D)}$ Using pseudo NMOS logic.

c. What is low power design in VLSI circuits?

d. Define scaling. Explain significance of scaling in VLSI circuits.

e. Explain working of 1-T DRAM cell.

Q.2 a. Explain CMOS inverter characteristics mentioning all regions of operation. What is the effect of changing W/L ratio on it? Explain with example. 10

b. Implement 4:1 mux using pass transistor logic. Explain advantages of using transmission gates. 10

Q.3 a. Derive equations for noise margin for CMOS invertor. 10

b. Explain working of 6-T SRAM cell. 10

Q.4 a. Explain clock generation networks and distribution networks used in VLSI circuits. 10

b. What is fast adder? Explain any one schemes for fast adder. 10

Q.5 a. Explain pseudo NMOS logic and hence implement 2 I/P NAND gate. 10

b. Explain various ESD protection schemes. 10

Q. 6 Write a short note on. 20

a. Barrel shifter

b. NOR based ROM array

c. Interconnect scaling

d. Level-1 and Level-2 MOS models.
