(6b) TE (SEM: VI) (Rev: 2012) (CBSGS) ETRX 10/5/16

Basic VLSI Design

Q.P. Code : 591600

(3 Hours) **[Total Marks :80**

N.B. : (1) **Question** No.**1** is compulsory.
(2) Attempt any **three** out of remaining.
(3) Assume suitable data wherever required.

1. (a) Draw and explain AND gate using pass transistor logic. **20**
(b) Explain drawhack of dynamic CMOS design.
(c) Draw and explain manchester carry circuit.
(d) What are various programming techniques used for EEPROM in Explain them in short.

2. (a) Draw 6T SRAM cell and explain it's read and write operation. **10**
(b) Define scaling ? Explain various types of scaling in detail. **10**

3. (a) Explain latch up condition in CMOS in detail. What are remedies to avoid latchup. **10**
(b) Give and explain the drawback of ripple carry adder. Explain 4 bit CLA adder with it's carry equations, logical network using dynamic CMOS logic. **10**

4. (a) Explain how ESD (electrostatic discharge) affect the MOSFET. Give and explain input protection circuits. **10**
(b) Give and explain interconnect scaling with its width, length, thickness and capacitances. **10**

5. (a) Explain various technique of clock generation. Discuss 'H' tree clock distribution. **10**
(b) Consider a CMOS inverter circuits with following parameters **10**

VDD = 3.3v VTon = 0.6v VTop = - 0.7v, $\mu_n C_{ox}$ = 60 μ A/v², $\left(\frac{W}{L}\right)_n$ = 8

$\mu_p C_{ox}$ = 20 μA/V², $\left(\frac{W}{L}\right)_p$ = 12. Calculate the noise margin.

6. Write a short note on **20**
(1) Sense ampliter
(2) Barrel shifter
(3) Interconnect parameters

Con.8159-16.