

Basic VLSI Design

QP Code : 5043

(3 Hours)

[ Total Marks : 80

- N.B. (1) Question No. 1 is compulsory.  
 (2) Solve any three questions from remaining questions.  
 (3) Assume suitable data if necessary.

1. Solve any four of the following :—

- (a) Explain the effect on drain current due to channel length modulation and velocity saturation. 5
- (b) Implement using CMOS inverters. 5  

$$F = \overline{A \cdot B} + C$$
- (c) Draw voltage transfer characteristic for CMOS inverter and explain all regions. 5
- (d) Give the read and write stability criteria for 6T RAM if the pull up transistors and replaced by resistors. 5
- (e) Explain low power design considerations. 5

- 2. (a) Compare pass transistor logic, NMOS logic and CMOS logic. 10
- (b) For equal rise and fall delay time assume  $\mu_n = 2 \mu_p$  draw an inverter equivalent circuit of 3 i/p NAND and 2 i/p XOR. 10

- 3. (a) Compare constant voltage and constant field scaling with their merits and demerits. 10
- (b) Write short note on clock generation, stabilization and distribution. 10

- 4. (a) Explain concept of carry look ahead adder with equation and how does it achieve better speed compared to ripple carry Adder. 10
- (b) Consider a CMOS inverter with following parameters 10  

$$\text{Nmos } V_{to, n} = 0.6 \text{ V } \mu_n C_{ox} = 60 \mu\text{A} / \text{V}^2 \text{ and } \left(\frac{W}{L}\right)_n = 8$$

$$\text{p mos } V_{to, p} = -0.7 \text{ V } \mu_p C_{ox} = 25 \mu\text{A} / \text{V}^2 \text{ and } \left(\frac{W}{L}\right)_p = 12$$
 Calculate the noise margin and switching threshold ( $V_{Th}$ ) of this circuit,  $V_{DD} = 3\text{V}$ .

- 5. (a) Implement 4 : 1 multiplexer using pass transistor logic. 10
- (b) Explain concept of charge sharing and charge leakage. 10

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6. Write a short notes on any **three** of the following :—

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- (a) Sense amplifier
  - (b) Array multiplier ( $4 \times 4$ )
  - (c) CMOS Latch up and it's prevention.
  - (d) Resistance and capacitance estimation.
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