T.E. Sem V Computer (CBGS). 24/11/14.
Microprocessor

QP Code :14858

(3 Hours) **[Total Marks : 80**

N. B. : (1) Q. 1 is **compulsory**.
(2) From remaining answer any **three** questions.
(3) Draw neat diagram wherever necessary.

1. (a) Draw and explain timing diagram for read operation in minimum mode of 8086. **5**
(b) Explain I/O related addressing mode of 8086. **5**
(c) Write down features of super SPARC processor. **5**
(d) Enlist the instruction pairing rules for U and V pipeline in Pentium. **5**

2. (a) Explain address translation mechanism used in protected mode of 80386. **10**
(b) Write assembly language program for 8086 to exchange contents of two memory blocks. **10**

3. (A) Design 8086 microprocessor based system with following specifications **10**
(a) Microprocessor 8086 working at 10 MHz in minimum mode
(b) 32 KB EPROM using 8 KB chips
(c) 16 KB SRAM using 4 KB chips
Explain the design along with memory address map.
(B) Explain how the flushing of pipeline problem is minimized in Pentium architecture. **10**

4. (a) Interface DMA controller 8237 with 8086 microprocessor. Explain different data transfer modes of 8237 DMA controller. **10**
(b) Differentiate between real mode and protected mode. **10**

5. (a) Draw & explain block diagram of 8259 PIC. **10**
(b) Draw a segment descriptor format and explain different fields. **10**

6. Write short note on any **four** :– **20**
(a) Code cache organization of Pentium.
(b) State the use of RF, TF, VM, NT, IOPL flag bits
(c) Data types supported by SPARC processor
(d) Advantages of memory segmentation in 8086.
(e) Maximum mode of 8086
(f) Control word register of 8255.
