SE MTRX | SEM-III | CBSGS | SUB:- D.E | DT- 02/00/2018.

Q. P. Code : 39633

(3 hours) Total Marks: 80

N.B.: (1) Question No. 1 is compulsory.
(2) Solve any **three** questions from remaining five questions.
(3) Draw neat diagrams and assume suitable data wherever necessary. Justify your assumptions.

1. (a) Explain stuck at '0' & stuck at '1' fault model. 20
(b) Explain Fan in, Fan out, Noise Margin, Propagation Delay, Power dissipation concepts of digital IC.
(c) Implement the following expression using 8:1 MUX.
$F(A,B,C,D) = \sum m(0,2,3,6,8,9,12,14)$
(d) Differentiate between SRAM and DRAM.

2. (a) Design & implement full subtractor using IC 74138. 10
(b) Write a VHDL code to design 1:8 demultiplexer. 10

3. (a) Design Mealy type sequence detector to detect a serial i/p **"110"**. 10
(b) Design a circuit with optimum utilisation of PLA to implement BCD to gray code converter. Specify the size of the PLA.. 10

4. (a) Design a 8-bit magnitude comparator using 7485. 10
(b) Design and explain universal shift register. 10

5. (a) What is Bush diagram? Design a mod 15 synchronous counter using T flip flops. 10
(b) Write a note on state diagram. 10
Determine the minimum state table equivalent and draw the reduced state diagram.

Present State	Next State		Output
	X=0	X=1	
A	B	C	1
B	D	C	0
C	F	E	0
D	E	B	1
E	B	C	1
F	C	E	0
G	F	G	0

6. Write short note on: 20
(a) Structural style of architecture modeling
(b) 2 i/p TTL NAND gate
(c) Frequency division in asynchronous counters

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