Dt-30/5/2017

QP Code : 13319

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question No. **1** is **compulsory**.
(2) **Solve** any **three** questions from remaining **five** questions.
(3) Draw neat **diagrams** and assume suitable **data** wherever **necessary**. Justify your **assumptions**.

1. (a) Explain current sourcing and current sinking when two standard TTL gates are connected. 5
   (b) Explain the problems faced by a ripple counter with a waveform. 5
   (c) Draw the architecture block diagram of Xilinx XC 9500 CPLD. 5
   (d) Write a note on two input TTL NAND gate. 5

2. (a) Write a note on VHDL. Write a VHDL code for a 8 : 1 Multiplexer. 10
   (b) Design a MOD 13 synchronous up counter using T flip flops. Write the truth table and draw the timing diagram. 10

3. (a) Design a 10-bit comparator using IC 7485. 10
   (b) Determine the minimum state table equivalent and draw the reduced state diagram : 10

Present State	Next State		Output	
	X = 0	X = 1	X = 0	X = 1
1	1	1	0	0
2	1	6	1	1
3	4	5	0	0
4	1	7	1	0
5	2	3	0	0
6	4	5	0	0
7	2	3	0	0

4. (a) Design a circuit with optimum utilization of PLA to implement the following functions : 10
   (i) $F1(A, B, C) = \Sigma m(0, 3, 4, 7)$
   (ii) $F2(A,B,C) = \Sigma m(1, 2, 5, 7)$
   (b) Design 16 : 1 multiplexer using 4 : 1 multiplexers. 10
   Implement the following using 8 : 1 MUX using only NAND gates
   $P(A, B, C, D) = \Sigma m(0, 1, 3, 4, 5, 7, 10, 12, 13) + d(2, 8)$

5. (a) Implement a sequence detector using Moore machine to detect a sequence . . . 101 . . . using D flip flop and logic gates. 10
   (b) Implement the following functions using only NAND gates :— 10
   (i) $f(A, B, C, D) = Lm(1, 2, 3, 4, 7, 11, 13) + d(9,15)$
   (ii) $f(W, X, Y, Z) = TTM (0, 6, 7, 8, 12, 13, 14, 15)$

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6. Write short notes on any **three** of the following :— 20
   (a) JTAG and BIST
   (b) Stuck at '0' and' 1' faults
   (c) SR Flip flop
   (d) Internal block diagram of IC 7490.
