Q.P. Code: 40985

(3 Hours) **[Total Marks: 80**

N.B.: (1) Question No. **1** is **compulsory.**
(2) Solve any **three** questions out of remaining **five.**
(3) Figures to **right** indicate **full** marks.
(4) Assume suitable **data** where **necessary.**

1. Solve any four out of five sub questions. [04 x 05=20]

a) Explain Von-Neumann Architecture.

b) Draw and explain 6 stage instruction pipeline.

c) What are the various functions performed by I/O module?

d) Differentiate between RICS & CISC.

e) Represent $(15.125)_{10}$ in IEEE 754 single precision floating point standard.

Q. 2. a) Multiply (- 5) and (2) using Booth's Algorithm. 10

b) Discuss various pipeline hazards with example. 10

Q. 3. a) Explain the register organization of a CPU. 10

b) Consider the string 8, 3, 9, 4, 9, 8, 5, 8, 3 ,9, 6, 7, 5, 4, 3, 9, 4, 9, 3 10

Find the page faults for 3 frames using FIFO, Optimal, & LRU page replacement policies.

Q. 4. a) Divide 18 by 5 using restoring division algorithms. 10

b) Explain Flynn's classification in detail. 10

Q. 5. a) Discuss the various characteristics of Memory. 10

b) Explain design of control unit w.r.t. micro-programmed and hardwired approach. 10

Q. 6. a) Explain different addressing modes with example. 10

b) What is the need of DMA? Explain its various techniques of data transfer. 10
