

Q.P. Code :23710

[Time: Three Hours]

[ Marks:80]

Please check whether you have got the right question paper.

- N.B:
1. Question.No.1 is compulsory.
  2. Solve any **three** questions out of remaining five questions.
  3. Assume suitable data if necessary
  4. Figures to right indicate marks

Q. 1 Attempt **any 4** sub questions.

- a) Define the terms Computer Organization and Computer Architecture. (05)
- b) Draw and explain single and double precision IEEE 754 binary floating point representation formats. (05)
- c) List and Explain important parameters significant in choosing a computer memory. (05)
- d) Draw and explain five stage instruction pipelining. (05)
- e) Explain Programmed I/O technique of Data transfer. (05)

- Q. 2
- a) Calculate the number of page hits and faults using FIFO, LRU and OPTIMAL page replacement algorithms for the following page frame Sequence: 5,6, 6, 3, 8, 5, 7, 8, 6, 5, 8, 5. (FRAME SIZE = 3). (10)
  - b) Draw and explain basic instruction execution cycle. (10)

- Q. 3
- a) Explain memory hierarchy of a computer. (10)
  - b) Describe Flynn's classification in detail. (10)

- Q. 4
- a) Describe different addressing modes. (10)
  - b) Draw the flowchart of Booths algorithm and multiply  $(6)*(-4)$  using Booths algorithm. (10)

- Q. 5
- a) Explain interrupt driven I/O technique of Data transfer. (10)
  - b) Explain hardwired approach to the design of a control unit. (10)

- Q. 6 Write notes on ( any three ) (20)
- a) Register Organization of a processor
  - b) Von Neumann architecture
  - c) Associative memory
  - d) Nano Programming
  - e) Pipeline Hazards

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