Q. P. Code : 37942

(3 Hours)   (Total Marks : 80)

Please check whether you have the right question paper.

N.B.:
1) Questions No. 1 is **compulsory**.
2) Solve **any three** question out of remaining **five** questions.
3) Assume suitable **data** if **necessary**.
4) **Figures** to the **right** indicate **full marks**.

1 Solve any **four** out of five :   (20)
   a) Explain Input and Output characteristics of CE configuration of BJT.
   b) Convert following decimal number to Binary, Octal, Hexadecimal and Gray code $(154)_{10}$.
   c) Design EX-OR gate using only NOR gates.
   d) Draw two truth tables illustrating the outputs of a full-adder, one table for the sum output
   e) Covert S – R filp-flop to D flip-flop.

2. a) Implement following using only one 8: 1 Multiplexer and few gates :   (10)
    $$f(A, B, C, D) = \sum m(1, 2, 3, 5, 6, 9, 10, 11, 14)$$

    b) Using Quine McCluskey Method determine Minimal SOP form for   (10)
    $$f(A, B, C, D) = \sum m(1, 3, 5, 6, 8, 9, 12, 14, 15) + \sum d(4, 10, 13)$$

3. a) Explain Collector to base bias Circuit with its stability factor.   (10)
    b) With neat diagram explain operation of ALU IC74181.   (10)

4. a) Design a Mod 10 synchronous counter using S-R Flip-flop.   (10)
    b) Minimize the following four variable logic function using K-map :   (10)
    $$f(A, B, C, D) = \sum m(0, 2, 3, 5, 6, 7, 8, 10, 11, 14, 15)$$ and design using only NAND gates.

5. a) Simplify following equation using Boolean algebra and Design using basic gates   (10)
    $$f(A, B, C) = A'B + BC' + BC + AB'C'.$$

    b) Explain Entity in VHDL and Write VHDL program for half subtractor circuit.   (10)

6. Solve the following (**Any Four**) :   (20)
    a) Explain working of Universal Shift Register.
    b) Working of T flip flop.
    c) Explain working of Differential Amplifier.
    d) Write VHDL program for EX-NOR gate.
    e) Explain working of Encoder and Decoder.

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