

ADC

Q.P. Code : 5229

(3 Hours)

[Total Marks :100

- N.B. : (1) Q.No 1 is compulsory
 (2) Solve any three questions out of remaining questions.
 (3) Assume suitable data if necessary.

1. Solve any five

(a) Convert

(i) $(174.03125)_{10}$ in octal number and $(DB.94)_{16}$ in binary(ii) Make subtraction using 2's complement method $(59)_{10} - (65)_{10}$

(b) Compare schottky barrier diode and PN junction diode

(c) Derive the relation between α and β .

(d) List the ideal characteristics of OPAMP

(e) Prove that NAND gate is universal gate.

(f) Convert T-FF to D-FF

20

2. (a) Draw block diagram of a shunt voltage regulator and explain the working

4

(b) Derive the expression for the stability factor 'S' of a voltage divider bias circuit

8

(c) Draw circuit diagram of differentiator using OPAMP and explain

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3. (a) Explain inverting summing amplifier using OPAMP. Derive the expression for output voltage.

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(b) $Y = ABC + \bar{B}CD + \bar{A}BC$ simplify this equation and realize using basic gates.

4

(c) Minimize the following expression using K-map

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$$Y = \sum m (1,2,9,10,11,14,15)$$

Implement the circuit using minimum number of gates

4. (a) Design an 8 bit comparator using IC 7485

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(b) Implement the following function using 8:1 Mux

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$$F(A, B, C, D) = \sum m (0,1,2,4,6,9,12,14)$$

(c) What is shift register? Mention different modes of operation of shift register.

8

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5. (a) What are advantages of VHDL
Write VHDL program for full adder 8
- (b) Design 4 bit synchronous up counter using T-FF 8
- (c) Draw the circuit of JK FF using NAND gates and write the truth table 5
6. (a) Design an astable multivibrator using IC 555 timer to generate an output of 1KHz with 60% duty cycle 5
- (b) Draw the circuit diagram of regulated power supply to produce an output voltage of +5V 5
- (c) Draw drain characteristics of n-channel JFET and explain various regions 5
- (d) What is excess 3 code? Why it is called self complementary code? 5