

Con. 9817-13.

GX-12167

(3 Hours)

[ Total Marks : 80

- N.B. :** (1) Question No. 1 is compulsory.  
 (2) Solve any **three** questions out of **remaining** questions.  
 (3) Assume **suitable** data if **necessary**.

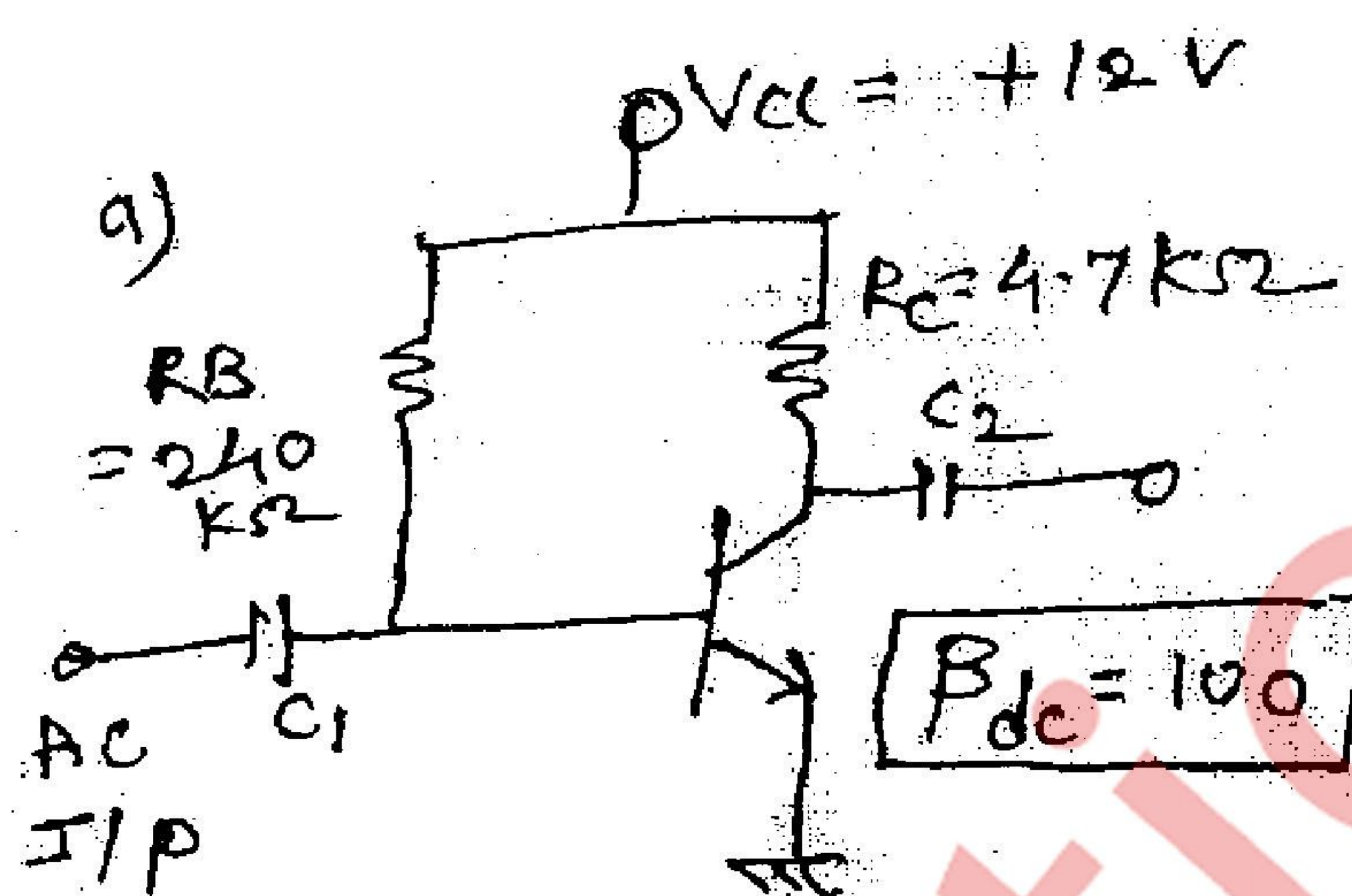
1. Solve any **four** :-

20

- Find out relations between  $\alpha, \beta$  and  $\gamma$  as current amplification factors for CE, CB, CC configurations.
- State ideal and practical characteristics of Op-Amp.
- Convert following decimal number to Binary, Octal, Herl-equivalent and gray code.
  - $(306.8)_{10}$
  - $(147.8)_{10}$
- Add  $(57)_{10}$  and  $(26)_{10}$  in BCD.
- Convert S-R filp-flop to D-flip-flop.
- Explain parallel input, serial output shift register.

2. (a) Determine the following for the fixed bias

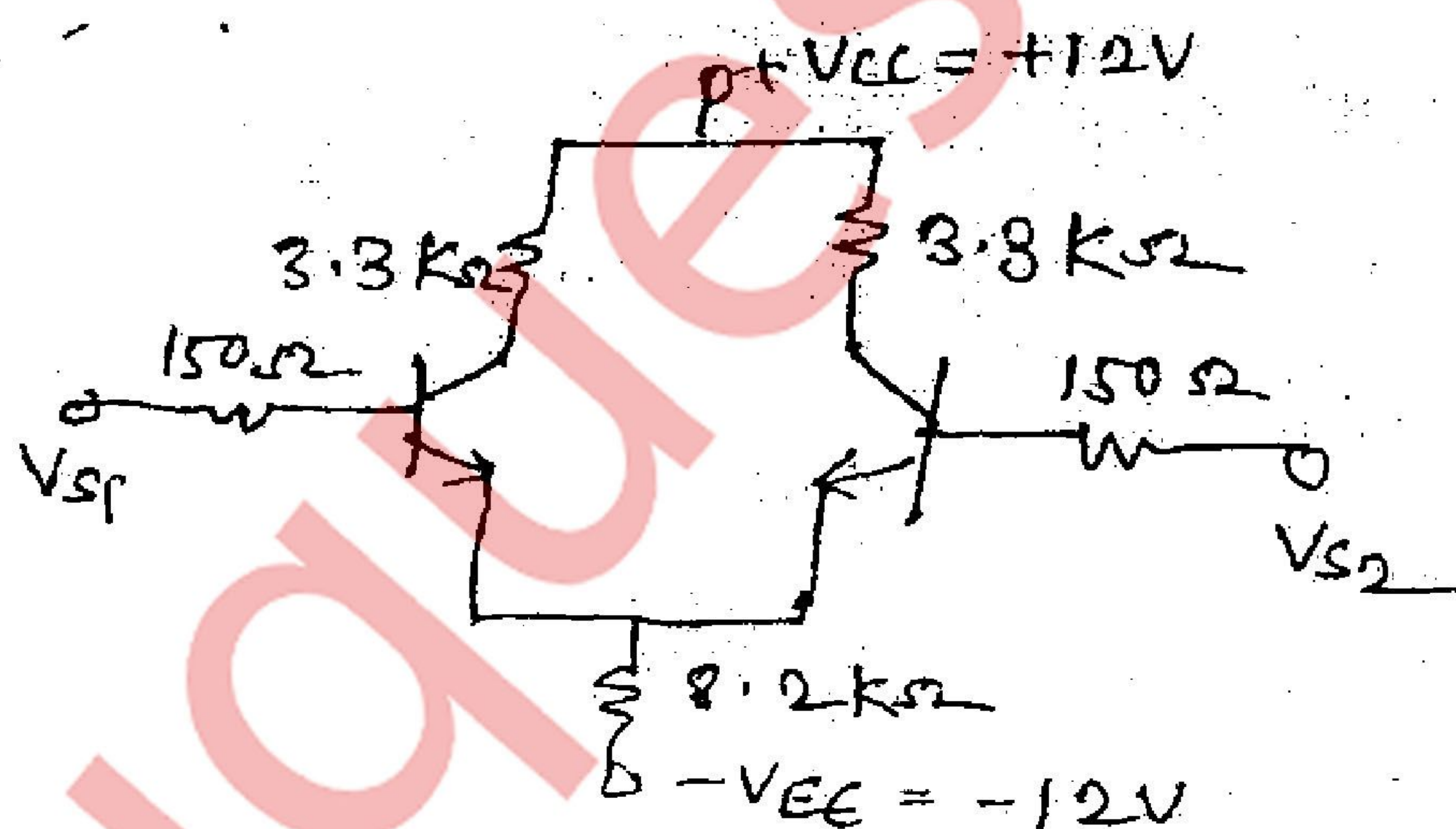
8



- $I_{BQ}$  and  $I_{CQ}$
- $V_{CEQ}$
- $V_B$  and  $V_C$
- $V_{BC}$

(b) For the differential amplifier as shown below calculate :-

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- Operating points
- Voltage gain
- Input Impedance
- Output impedance

(c) Design a circuit to  $V_0 = 15(V_1 - V_2)$  where  $V_1$  and  $V_2$  are input voltages to Op-Amp.

4

- What are different methods used to improve CMRR in differential amplifier?
- Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to about 5 KHz.
- Explain Instrumentation amplifier using 3 Op-Amps.

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4. (a) Design an astable multivibrator for an output frequency of 1KHz and duty cycle 40 %. **6**
- (b) Minimize the following expression using K-map and realize using the gates. **6**
- $$Y = \sum m (1, 2, 9, 10, 11, 15, 15)$$
- (c) Design 2 - Bit magnitude comparator using basic gates. **8**
5. (a) Implement the following function using 8 : 1 MUX **6**
- $$f (A, B, C, D) = \sum m (2, 4, 5, 7, 10, 15)$$
- (b) Implement full adder using demultiplexer. **6**
- (c) Design the divide by 7 (mod-7) asynchronous up-counter using J-K flip-flop. **8**
- Also state difference between synchronous and asynchronous counter.
6. (a) Explain universal shift register and its applications. **6**
- (b) Explain VHDL. **4**
- (c) What is Zener shunt regulator? Explain and derive stability factor. **4**
- (d) Realize following using only NAND gates. **6**
- $$Y = (AB + BC) C.$$

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