Time: 3 Hours   **Total Marks: 80**

N. B.1) Question No. 1 is compulsory **(Any Four).**
   2) Answer any **3** questions from the remaining **5** questions.
   3) Assume suitable data wherever necessary.

Q1 (a) Write a short note on zero crossing detector.   **20**
     (b) Describe the term loading effect with suitable example.
     (c) The resistors in a bridge are given by R1=R2=R3=120 Ω and R4 = 121 Ω. If the supply voltage is 10V. Find the offset voltage.
     (d) Draw and explain Sample and Hold circuit.
     (e) Design a ±12V power supply using IC 78xx.

Q2 (a) Define multivibrator? Explain astable multivibrator using IC 555 and also design astable   **20** multivibrator for 50% duty cycle.

     (b) Draw and explain circuit for ideal integrator with waveforms. Discuss the problems associated with ideal integrator and draw the circuit diagram for practical integrator.

Q3 (a) A thermistor is to monitor room temperature. It has a resistance of 3.5 KΩ at 20°C with   **20** a slope of -10%/°C. The dissipation constant is P_D=5mW/°C. It is proposed to use the thermistor in the divider as shown below to provide a voltage of 5.0V at 20°C. Evaluate the effect of self-heating. (R_2= Thermistor; R_1=3.5KΩ)
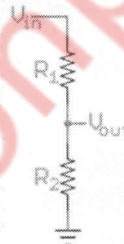
     (b) Draw and explain the principle and construction of metal strain gauges. What is the signal conditioning associated with it.

Q4 (a) Explain successive approximation analog to digital converter. Find ADC output for a 4-   **20** bit converter to a 2.87V input, if the reference is 5V.

     (b) Design a second order high pass filter for cutoff frequency equal to 1.5 KHz.

Q5 (a) A potentiometric displacement sensor is to be used to measure work-piece motion from   **20** 0 to 10 cm. The resistance changes linearly over this range from 0 to 1KΩ. Develop signal conditioning to provide a linear, 0- to 10-V output.

     (b) Explain the absolute value circuit with labelled circuit diagram and its waveform.

Q6 (a) Draw and explain the principle and construction of RTD. What is the signal   **10** conditioning associated with it.
     (b) Phase Locked loop   **5**
     (c) SMPS   **5**

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