INST/CBGS/III/~~Apply Physics-II~~ DE | 25-11-2016

Digital Electronics **Q. P. Code : 550601**

(3 Hours) **(Total Marks : 80)**

N.B. (1) Question no 1 is compulsory.
(2) Attempt any three questions from the remaining questions
(3) Figures to the right indicate full marks.
(3) Assume suitable data wherever necessary.

1. Answer the following (**any four**) **20**

(a) Convert: (i) $(21D.2F)_{16}$ to $(?)_{10}$. (ii) $(67)_{10}$ to $(?)_{BCD}$.
(b) What is a debounce switch? Why is it used in digital switching circuits? Explain.
(c) State and prove DeMorgan's theorems.
(d) Design half subtractor using logic gates.
(e) Simplify with k-map & implement with logic gates $f = \Sigma m\,(2, 3, 4, 5, 12, 13)$.

2. Perform. **20**

(a) Perform the following:-
(i) Subtract $(CB2)_{16}$ & $(972)_{16}$ use the 16's complements method.
(ii) Write the Hamming code for data 1101.
(b) Simplify using Boolean laws & implement with logic gates.
(i) $f = \overline{A}BCD + A\overline{B}CD + \overline{A}B\overline{C}D + \overline{A}BC\overline{D}$
(ii) $f = (AB.(\overline{\overline{C} + D}).(\overline{AB})$

3. (a) Convert SR flip flop to D flip flop & TFF. **10**
(b) Design & implement with gates a parity generator circuit for odd parity. **10**

4. (a) Design a MOD-6 ripple counter using JKFF draw o/p waveforms for each flip flop. **10**
(b) Design & implement a full odder circuit using a 3:8 Decode. **10**

5. (a) Explain with a neat diagram working of SISO shift register. Draw necessary timing diagram. **10**
(b) Simplify following using k-map & implement using logic gates. **10**
$f = \Sigma m(0,3,5,7,8,11,12,15)+d(2,13)$

6. Write a short notes on:- (any four) **20**
(1) ALU
(2) Dynamic RAM cell.
(3) PAL & PLA.
(4) FPGA
(5) Schottky clamped TTL.

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