S-E (Sem.-III) INST

K. G. C. E. EXAM KARJAT, RAIGAD

Digital Electronics-I / 20-11-14

QP Code **14547**

(3 Hours) [Total Marks : 80

N.B. : (1) Question No. **1** is **compulsory**. Attempt any **3** qustions out of remaining **5** questions.
(2) **All** questions carry **equal** marks.
(3) Assume **suitable** data is **necessary**.

1. Attempt any **four** :— 20
   (a) Explain difference between synchronous and asynchronous counter.
   (b) Explain gray code and its application in brief.
   (c) Design SR slip slop using only NOR gates.
   (d) Design Half subtractor using logic gates.
   (e) Implement 8 : 1 MUX using two 4 : 1 MUX.

2. (a) Perform following operations :— 10
   (a) $(3\ FD{\cdot}1E)_{16} \rightarrow (?)_{10}$
   (b) $(119{\cdot}27)_{10} \rightarrow (?)_{8}$
   (c) $(110101100111{\cdot}1010)_2 \rightarrow (?)_{10}$
   (d) 21 – 39 using 2's complement
   (e) $(168)_H \times (32F)_H$

   (b) Prove that— 10

   (i) $A\left[B+C\left(\overline{AB+AC}\right)\right]=AB$

   (ii) $A+\overline{A}B+\overline{A}\,\overline{B}C+\overline{A}\,\overline{B}\,\overline{C}D=A+B+C+D$

3. (a) Minimize following using k–map and implement using logic gates. 10
   $f = \Sigma\ m\ (0, 1, 3, 5, 9, 12) + d\ (2, 4, 6, 7)$
   (b) Design 2 bit magnitude comparator. 10

4. (a) Implement following using 8 : 1 MUX. 10
   $f = \Sigma\ m\ (0, 1, 3, 4, 5, 9, 10, 12, 13, 15)$
   (b) Design full adder using 3 : 8 decoder. 10

5. (a) Convert SR flip flop to JK flip flop. 10
   (b) Design MOD–11 asynchronous counter using JK flip flop. 10

6. Write short note on any **four** :— 20
   (a) Ring Counter
   (b) Logic family Comparison
   (c) ALU
   (d) PLA and PAL
   (e) Hamming Code.

GN-Con: 6454-14.