(3 Hours) **[Total Marks: 80]**

N.B: (1) **Question No. 1** is **compulsory**.
(2) Attempt any **THREE** questions from remaining.
(3) **Figures** to the **right** indicate **full marks**.
(4) Assume suitable **data** if **necessary**.

1. Answer the following: - [20]
   (a) Implement EX- OR logic gate using NAND gates.
   (b) Explain Fan-In and Fan-Out of digital ICs.
   (c) Explain the working of SR flip flop? What is meant by edge triggering?
   (d) Implement f (ABC) = ∑m (1,2,5) using 4:1 MUX.

2. (a) Prove the following using Boolean algebra. [10]
   i) $(A+\bar{B}+AB)(A+\bar{B})(\bar{A}B) = 0$
   ii) $\bar{A}BC + A\bar{B}C + AB\bar{C} + ABC = AB + AC + BC$
   (b) Perform-: i) $(24)_8 - (10)_8$ ii) $(64)_{16} + (33)_{16}$ [05]
   (c) Convert: [05]
   i) $(9CD)_{16} = (?)_{10}$ ii) $(0.42)_{10} = (?)_2$

3. (a) Design a 4 bit BCD adder using IC 7483. [10]
   (b) Design two-bit magnitude Comparator using logic gates. [10]

4. (a) Design 3 bit synchronous counter using JK flip- flop. [10]
   (b) Explain with a neat diagram working of SISO shift register. Draw necessary timing diagram. [10]

5. (a) What is FPGA? What are its salient features? [05]
   (b) What are the merits and demerits of TTL family? [05]
   (c) Design and implement a full subtractor circuit using 3: 8 Decoder. [10]

6. Write note on: - **(Any Four)** [20]
   (a) Hazards and Hazard elimination.
   (b) PAL and PLA.
   (c) Advantages of 2's complement number representation.
   (d) ASCII Code.
   (e) Basic dynamic RAM Cell.

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