E] Sem-III - Choice Based / INST / Analog Electronics /

Nov-2017.

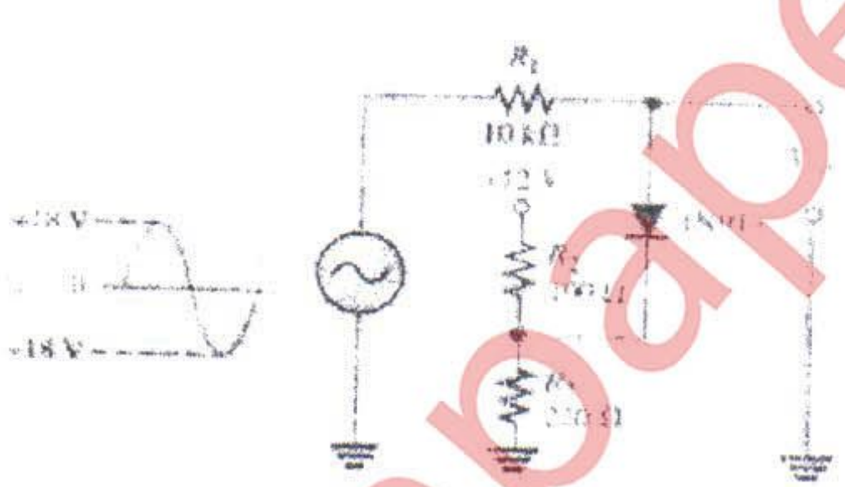
QP Code : 25991

Max. Time: 3 hr

Max. Marks: 80

Q.1 is compulsory (any Four). Attempt any 3 from Q.2 to Q.6

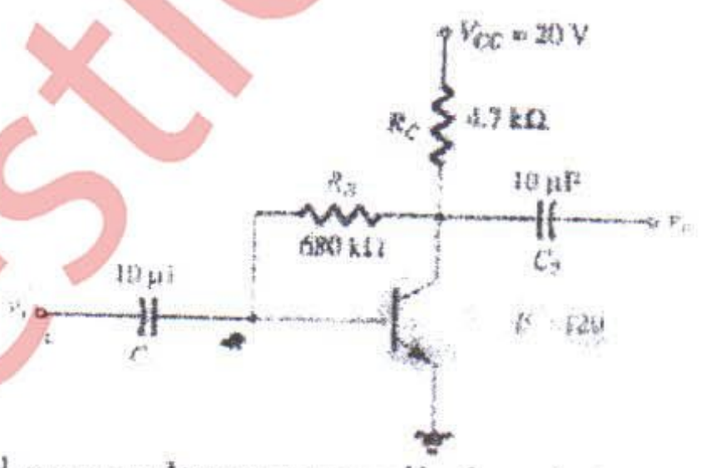
1(a) Describe the output voltage waveform for the diode limiter shown below (5)



1(b) Define a filter. How are filters classified? (5)

1(c) Explain Thermistor compensation with circuit diagram (5)

1(d) For the network of Fig. shown below determine I_C and V_{CE}, V_B, V_c



1(e) How FET be employed as a voltage controlled resistor. (5)

2(a) Determine the minimum value of R L to ensure that the Zener diode is in the "on" state (10)

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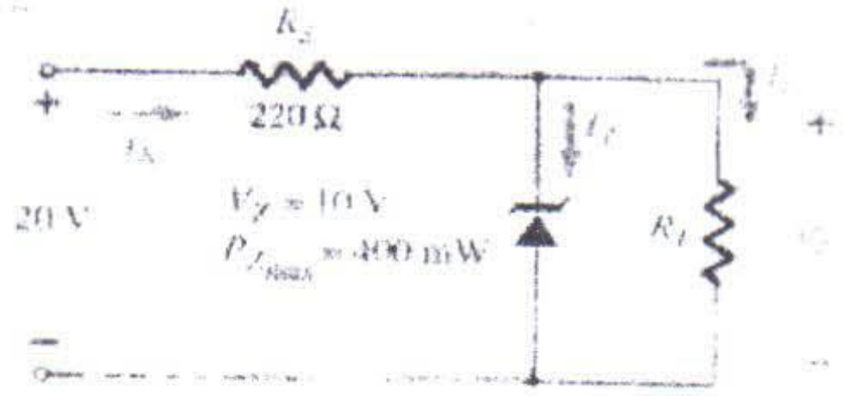
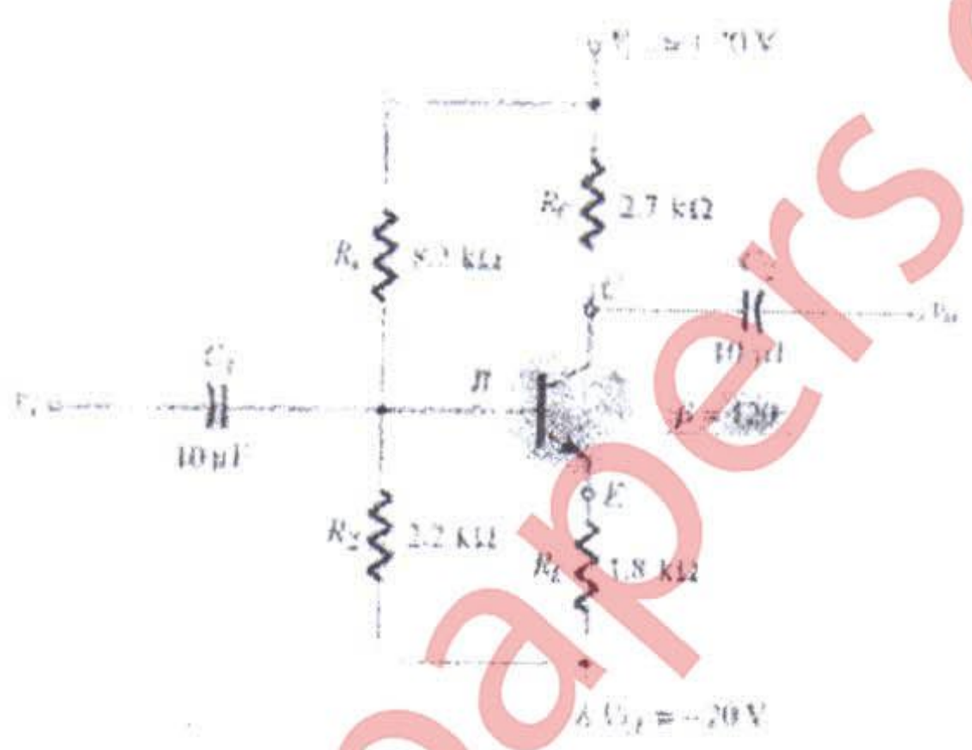


2(b) Compare class A, class B power amplifiers based on the output waveform for collector current, linearity, distortion and efficiency. (10)

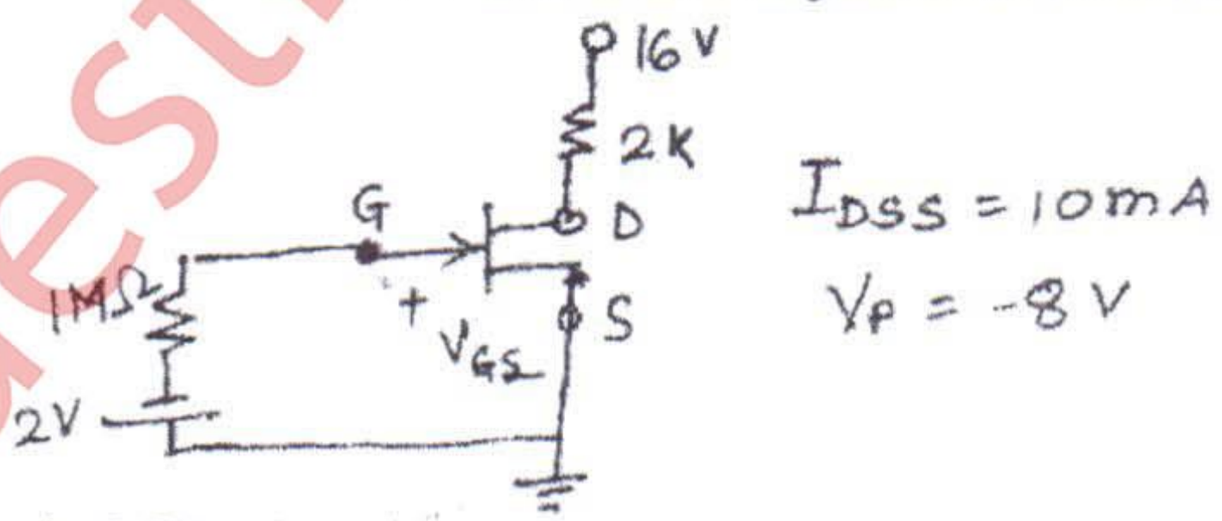
3(a) Determine V_C and V_B for the network of fig. shown below. (10)



3(b) Derive the expressions for the I_B, I_C and V_{CE} for emitter bias configuration of BJT. (10)

4(a) Explain the structure, operation and current-voltage characteristics of Enhancement type MOSFET. (10)

4(b) Determine V_{GS}, I_D, V_{DS} for the fixed Bias configuration as shown if fig below (10)



5(a) Using standard 5%resistances, design a circuit such that (10)

$$V_0 = -2(3v_1 + 2v_2 - 4v_3)$$