Paper / Subject Code: 51202 / Electronics Devices and Circuits-I

S.E. SEM - III / ELTL / CHOICE BASED / NOV 2018 / 28.11.2018

QP : Code : 25071

(3 Hours) [Total Marks : 80

Note: 1) Question no. 1 is compulsory.

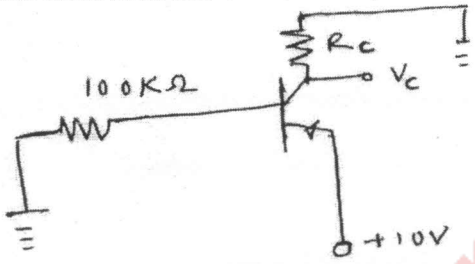
2) Solve any three questions out of remaining.

3) Fig. to the right indicates maximum marks.

4) Assume suitable data wherever necessary but justify the same.

Q1. Solve any five. (5x4 = 20)

a) Determine the value of Rc such that Vc = 5V and β = 50.

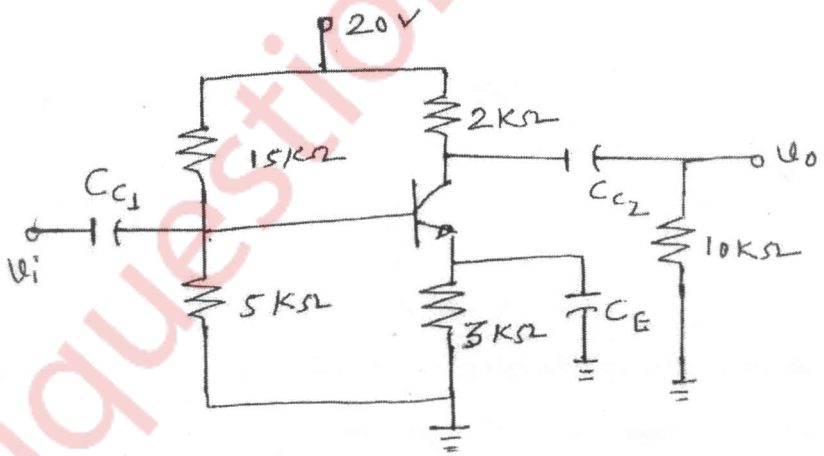


b) State and explain Miller's Theorem.

c) Design a self bias circuit using JFET for I_D = 3mA, V_{DD} = 20 V and V_{DS} = 0.6 V_{DD}. (I_{DSS} = 8 mA, V_P = -4V)

d) Explain various types of capacitors.

e) Determine the values of coupling capacitors C_{C1} and C_{C2} if r_Π = 1.5KΩ, β = 120 and f_L=20Hz.



f) Explain concept of zero temperature drift in JFET.

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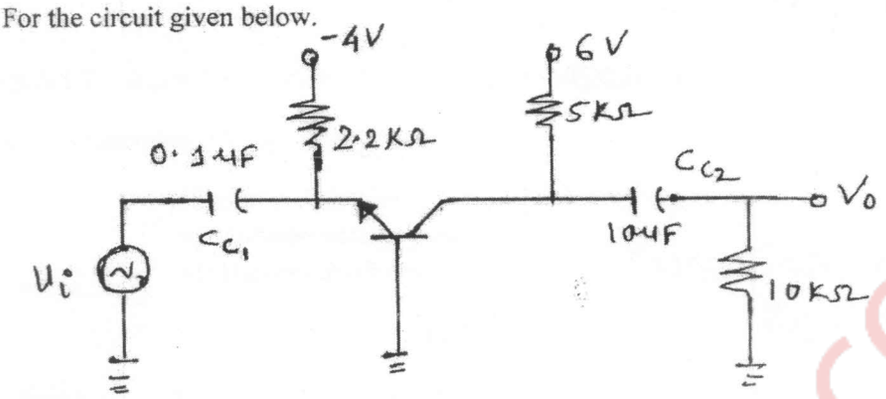
Q2. A) Calculate 1) I_{BQ} , I_{CQ} 2) g_m, r_Π 3) Small signal voltage gain **10**

For the circuit given below.



Take $\beta = 110$

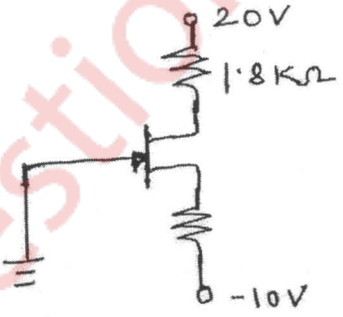
Q2 B) Explain the concept of LC filter in power supply circuit and hence derive expression for ripple factor of LC filter. **10**

Q3 A) Explain concept of shunt Zener regulator. For a shunt Zener regulator giving output voltage of 10 V and load resistance varying from 5KΩ to 10KΩ, Vin is varying between 18V to 22V. **10**

Find Rs, Pzmax, Sv and Ro.

Assume Rz = 4Ω and Izmin = 50μA.

B) Determine I_{DQ}, V_{GSQ}, V_{DSQ} if I_{DSS} = 9mA and V_P = -3V for the circuit given below. **10**



Take $R_S = 1{\cdot}5\ K\Omega$

Q4 A) Design capacitive filter with FWR using two diodes with ripple factor less than 5%. **10**

Output voltage is 24V and load current 200mA. The input line voltage of 230V/ 50Hz Is available.

B) Determine the values of biasing components for a CE configuration if Vcc = 12V, V_{CE} = 6V, Rc=1KΩ, V_{BE} = 0.6V, β = 180 for the following circuit. **10**

i) Fixed bias without R_E

ii) Voltage Divider bias with V_{RE} = 10% of Vcc and S_I = 8

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Q5 A) For JFET if I_{DSS} = 6 mA, V_P = -6V rd =∞, Cgd = 4pF, Cgs = 6pF, Cds = 1pF **15**

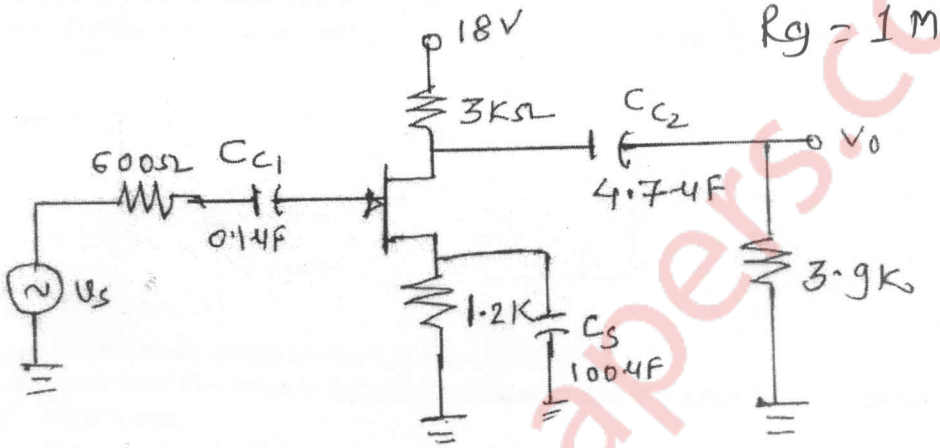
Determine i) V_{GSQ} ii) I_{DQ}

iii)gmo iv) gm

v) Midband voltage gain Av

vi) Higher cut off frequency

Take Gate resistance
Rg = 1 MΩ



B) Explain high frequency ∏ equivalent model of common emitter BJT. **5**

Q6. Design single stage CS amplifier using mid-point biasing method for voltage gain of 12, **20**

F_L =20 Hz, R_L = 10KΩ, Vo = 3.5V

(Use JFET parameters I_{DSS} = 7mA, V_P = -2.5V, gmo = 5600μ℧, rd = 50KΩ)