**Q.P. Code : 545402**

**(3 Hours )** **[ Total Marks : 80**

**N.B. :** (1) **Question No. 1** is compulsory.
(2) **Attempt any 3** questions from Q.2 to Q.6.
(3) Figures to the **right** in the bracket indicate **full** marks.
(4) Assume suitable data if necessary.

**1.** a) Compare Combinational circuits with Sequential circuits. **5**
b) Compare Synchronous counter with Asynchronous counter. **5**
c) Compare Moore machine with Mealy machine. **5**
d) Compare SRAM with DRAM. **5**

**2.** a) Implement the following Boolean equation using single 4:1 MUX and few logic gates : $F(A,B,C,D) = \Sigma\, m(0, 2, 5, 6, 7, 9, 12, 15)$. **10**
b) State and prove the De Morgan's theorem. **5**
c) Implement $Y = A + \overline{B}C$ using only NOR gates. **5**

**3.** a) Draw a neat circuit of BCD adder using IC 7483 and explain. **10**
b) Using Quine McClusky method, minimize the following: **10**
$F(P,Q,R,S) = \Sigma\, m(0,1,2,3,5,7,8,9,11,14)$.

**4.** a) Design synchronous counter using D type flip flops for getting the following sequence: $0 \rightarrow 3 \rightarrow 1 \rightarrow 5 \rightarrow 6 \rightarrow 0$. **10**
Take care of lockout condition.
b) Convert JK type flip flop into D type flip flop. **5**
c) Write $(27)_{16}$ into its BCD code and Octal code. **5**

**5.** a) Write the VHDL code for 3-bit up-down counter with negative edge triggered clock and active low Preset and Clear terminals. **10**
b) Compare TTL with CMOS logic families. **5**
c) Draw the internal logic diagram of Programmable Logic Array (PLA). **5**

**6.** a) What is shift register? Explain any one type of shift register. Give its application. **10**
b) Design a Mealy type sequence detector circuit to detect a sequence 1011 using D type flip flops. **10**

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