Q. P. Code : 20753

Time : 3 Hours **Total Marks: 80**

N.B. 1. Question No. 1 is **Compulsory**
2. Out of remaining questions, attempt **any three**
3. **Assume** suitable data if required
4. Figures to the right indicate **full marks**

1. (a) Compare SRAM and DRAM [5]
   (b) Compare Mealy and Moore machine [5]
   (c) Compare TTL and CMOS Logic [5]
   (d) Compare PLA with PAL [5]

2. (a) Prove that NAND and NOR Gates are universal Gates [10]
   (b) Design a full subtractor and implement using logic Gates [10]

3. (a) Design a 4 bit Binary to Grey code converter [10]
   (b) Implement the given function using 8:1 Multiplexer [10]
   $F(A, B, C, D) = \sum m(0, 1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 13)$

4. (a) Explain 4-bit asynchronous up counter with proper timing diagram [10]
   (b) Write a VHDL program to design a 4:1 Mux [10]

5. (a) Minimize the following expression using Quine McClusky Technique [10]
   $F(A,B,C,D) = \sum m(0, 1, 2, 3, 5, 7, 9, 11,15)$
   (b) Convert JK FF to T FF and SR FF to D FF [10]

6. (a) Design synchronous mod 5 counter using T FF [10]
   (b) Write a note on CPLDs [10]

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