S.E. EXTC – Sem 3 (CBGS). 20/11/14.

AE–I

(Analog Electronics-I).

QP Code : 14553

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question No.1 is compulsory.
(2) **Attempt** any **three** from remaining questions.
(3) **Assume suitable** data if required and mention the same in answer book.

1. Attempt any **five** :— **20**

(a) The PNP transistor shown in Fig la has β=50. Find the value of Rc to obtain Vc = +5V. What happens if transistor is replaced with another transistor having β=100.

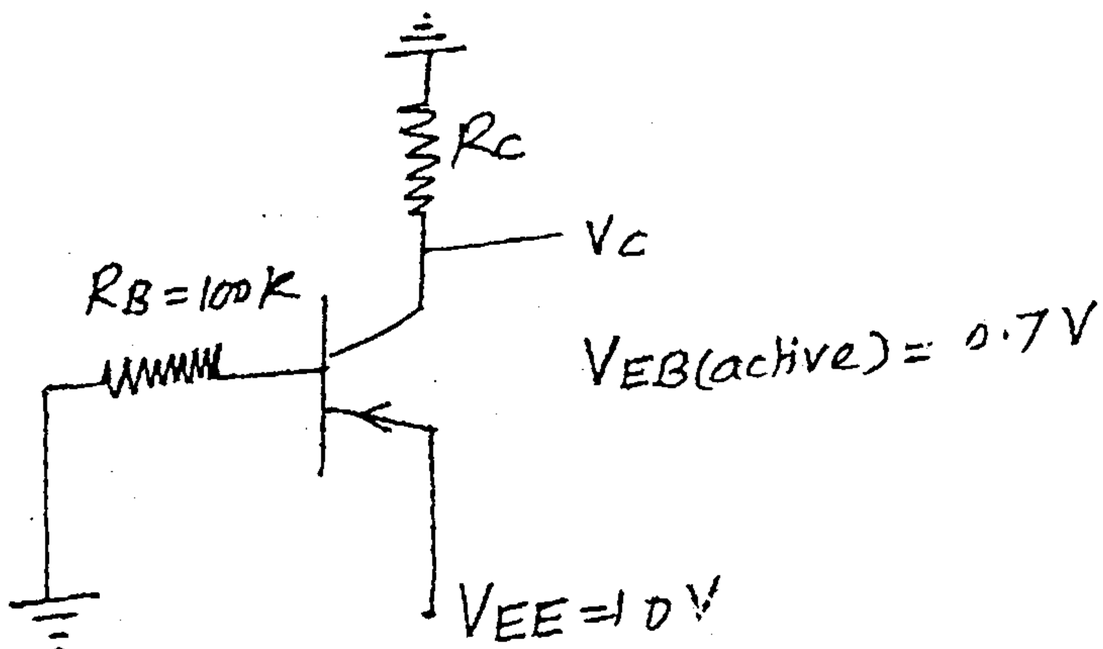

Fig 1a.

(b) Draw small signal model of JFET and explain significance of each parameter.
(c) Why common collector amplifier is used as buffer. Why buffers are required.
(d) Write down current equation of diode and explain significance of each parameters.
(e) For the circuit shown in Fig le. Find I_{DS} and V_{DS} if V_{RS}=1.5 V.

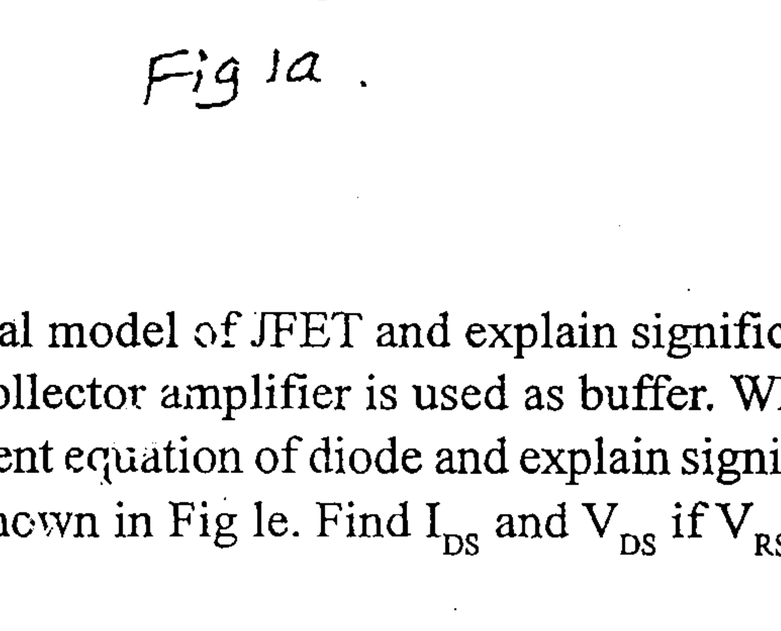

Fig 1e.

(f) Compare Collpit's and Clapp's oscillator.

2. (a) Explain working of n-channel EMOSFET with the help output characteristics, showing clearly effect of channel length modulation. Given equation of drain current in linear and saturation current along with conditions. **10**

(b) Design JFET circuit with voltage divider biasing as shown in Fig 2b with JFET parameters I_{DSS}=12mA, V_P= -3.5V and λ=0. Let R_1+R_2=100K, I_{DSQ} = 5mA and V_{DSQ}=5V. **10**

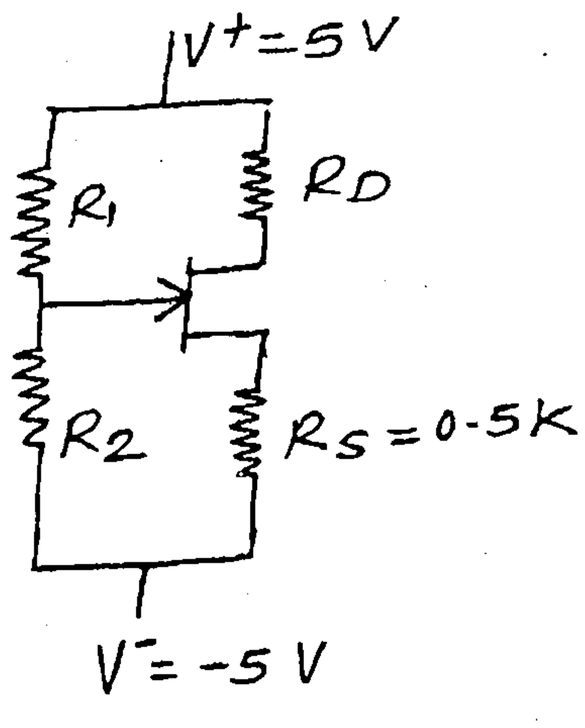

Fig 2b

3. (a) Draw circuit diagram of common emitter amplifier with voltage divider bias with bypassed emitter resistance and derive expression for voltage gain, current gain, input resistance, output resistance using hybrid-π model which includes early effect. **10**

(b) In n-channel E-MOSFET **10**

(i) Substrate doping $N_A=10^{16}$ cm^{-3}

(ii) Polysilicon Gae doping $N_D=10^{20}$ cm^{-3}

(iii) Gate oxide thickness tox =0.5 μm

(iv) Oxide positive charge interface density=$4x10^{10}$cm^{-2}

(v) Charge of electron= $1.6x10^{-19}$col

(vi) Permittivity of free space $\epsilon_0=8.85x10^{-14}$ F/cm.

(vii) Dielectric constant of Si=11.9

(viii) Dielectric constant of $Si0_2$ =3.9

Find zero bias threshold voltage (V_{TO})

4. (a) Explain the working of wien-Bridge Oscillator. Derive the expression for frequency of Oscillation and the value of gain required for sustained oscillation. 10

(b) For the circuit shown in Fig 4b, assume β=100. 10

(i) Find thevenin's equivalent voltage V_{TH} and resistance R_{TH} for base circuit.

(ii) Determine I_{CQ} and V_{CEQ}

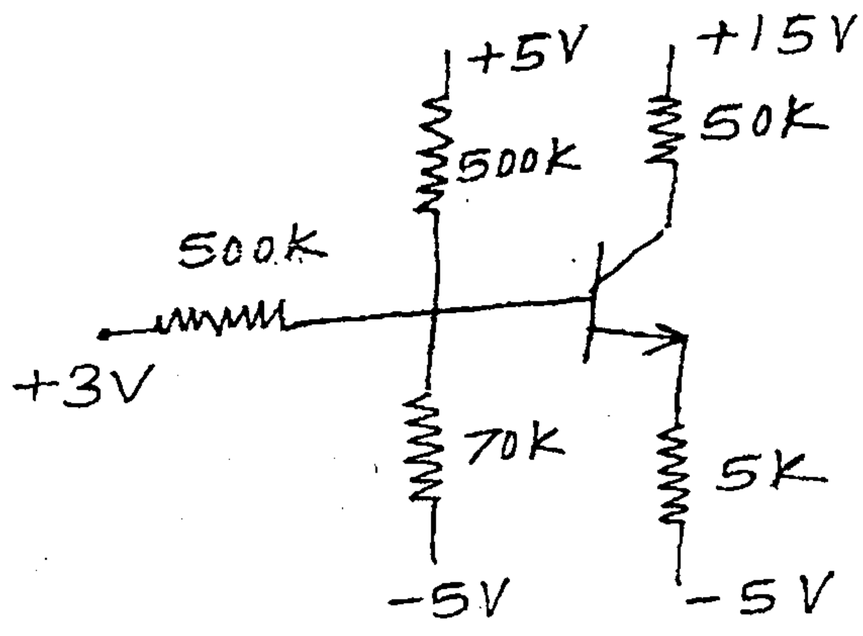

Fig 4b.

5. (a) Draw a required diode clamper circuit to generate the output v_o to from the input v_I as shown in Fig 5a if 10

(i) $V\gamma = 0V$

(ii) $V\gamma = 0.7V$. Where $V\gamma$ is cutin voltage of diode.

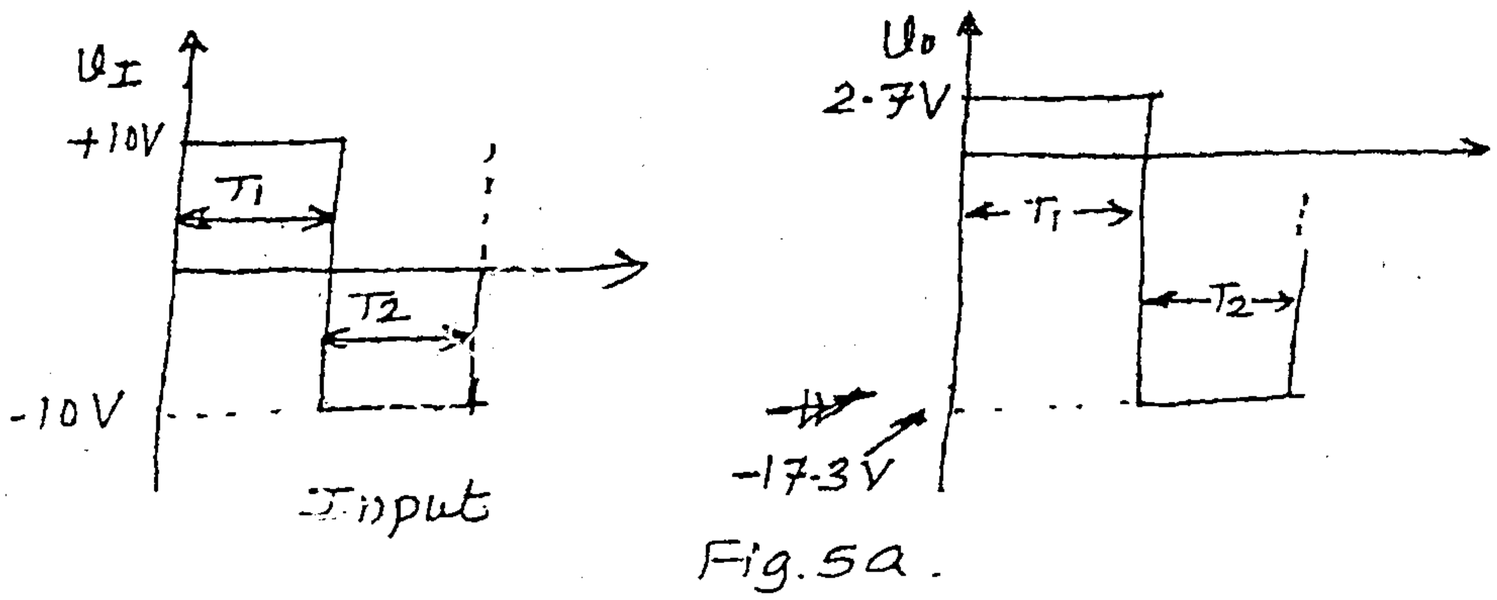

Fig.5a.

(b) What are different biasing techniques used to bias D-MOSFET and E-MOSFET. Explain with the help of appropriate circuit diagrams. **10**

6. Write short notes on any **four** :— **20**
   (i) Hybrid-π model of BJT
   (ii) Twin-T oscillator
   (iii) AC and DC load line.
   (iv) Construction and operation of photodiode.
   (v) MOS capacitor.
