Q.P. Code :10402

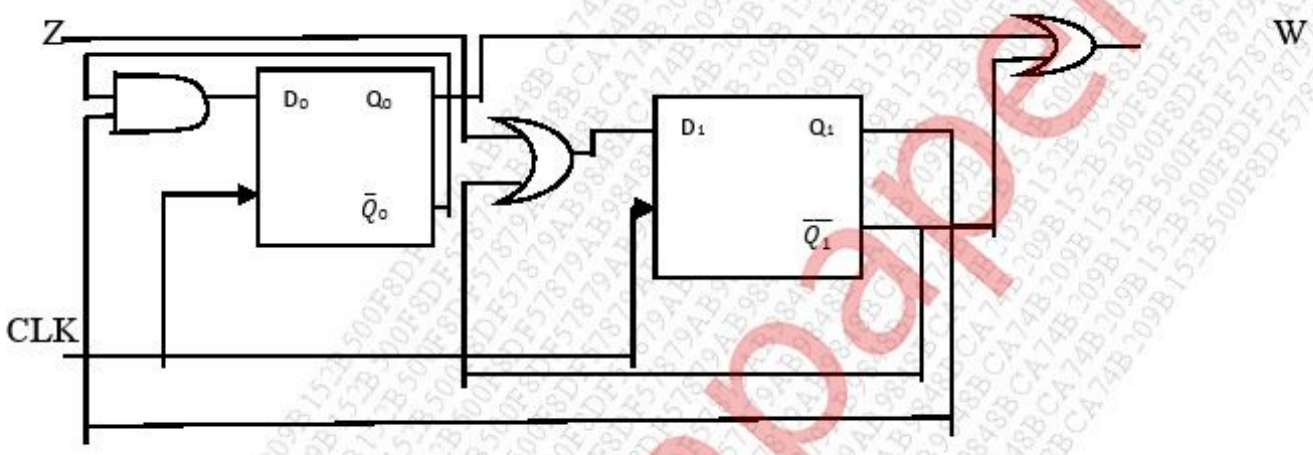
[Time: 3 Hours] **[Marks:80]**

Please check whether you have got the right question paper.

N.B: 1. Question No.**1** is **Compulsory**
2. Solve any **three** from the remaining **five** questions.
3. Draw neat **logic diagram** and assume **suitable data** wherever necessary.

Q.1 a. Two inputs TTL NAND gate **05**
b. Explain ring counter **05**
c. Draw truth table and logic diagram of Full Subtractor using half Subtractors and gates **05**
d. Explain the characteristics parameters of logic families **05**

Q.2 a. Analyze the clocked synchronous machine given below. Write excitation equations, excitation/transition table and state/ output table (Use state names A-D for Q1-Q-2=00-11) **10**



b. Design 1 digit BCD adder using IC 7483 and perform $(1010)_{BCD}+(1100)_{BCD}$ **10**

Q.3 a. Design a mealy sequence detector to detect----0100---- using D flip-Flops and logic gates **10**
b. Design a circuit with optimum utilization of PLA to implement the following functions **10**
$P=\Sigma m$ (1,3,8,10,10,15)
Q=Σ m(0,1,5,7,9,12,14)
R= Σ m(0,2,5,8,9,11)

Q.4 a. Implement following function using 4:1 MUX and NAND gates **10**
P(A,B,C,D)=Σm(1,2,6,7,8,10,13,14)
b. Explain IC 74194 working in detail with applications **10**

Q.5 a. Use K-map to reduce following function and then implement it by NOR gates. **10**
$F=\pi M(0,1,4,7,8,11,12,14)+d(2,5,6)$
b. Eliminate redundant states and draw the reduced state diagram **10**

Present state	Next State		Output Y
	X=0	X=1	
A	B	C	1
B	D	C	0
C	F	E	0
D	E	B	1
E	B	C	1
F	C	E	0
G	F	G	0

Q.P. Code :10402

Q.6 Write short notes on any three **20**

1. Master slave JK Flip Flop
2. Write a VHDL code for full adder
3. Stuck at '0' and '1' faults
4. CPLD and FPGA architecture block diagram