SE/Sem III/CBSGS/ETRX/DCD/7-12-2017

QP CODE : 22982

(3 Hours) Marks : **80**

NB : (1) Question **No.1** is **compulsory.**
(2) Out of remaining questions, attempt **any three** questions.
(3) Assume suitable data, wherever necessary.

1. (a) Draw Master slave JK flip flop **5**
(b) Describe ring counter operation with the help of logical diagram **5**
(e) Use half subtractors and gates to realize the Full Subtractor **5**
(d) Compare Moore and Melay machines **5**

2. (a) Design 2 bit comparator and draw its logical diagram **10**
(b) Design 1 digit BCD adder using IC 7483 and perform $(0011)_{BCD} + (1100)_{BCD}$ **10**

3. (a) Use 4:1 MUX and gates to implement the following function **10**
$Y(P,Q,R,S) = \sum m(0,3,4,6,9,11,12,14,15)$
(b) Explain the working of shift register IC 74194 in detail with applications. **10**

4. (a) Design a mealy sequence detector to detect ---1001--- using D flip-flops and logic gates **10**
(b) Design a circuit with optimum utilization of PLA to implement the following functions . **10**
$A = \sum m(1, 2, 6, 8, 11, 13, 15)$
$B = \sum m(0, 3, 5, 8, 9, 12, 14)$
$C = \sum m(0, 2, 4, 7, 10, 11)$

5. (a) Use K-map to reduce following function and then implement it by NOR gates. **10**
$F = \pi M(1, 2, 4, 7, 8, 11, 13, 15) + d(0, 5, 9)$
(b) Eliminate redundant states and draw the reduced state diagram. **10**

Present State	Next State		Output
	X = 0	X = 1	Y
A	B	D	1
B	C	E	0
C	E	F	1
D	E	B	0
E	D	C	0
F	B	D	1

6. Write short notes : **20**
(a) Universal shift register
(b) Johnson 4-bit counter
(c) Stuck at '0' and '1' faults
(d) Explain the characteristics parameters of logic families.

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