QP Code :14602

(3 Hours) [Total Marks : 80

N.B.: (1) Question No. 1 is Compulsory.

(2) Solve any **Three** from remaining **Five** questions.

(3) Draw **neat** logic diagram and assume suitable data wherever necessary.

Q 1 (a) Interfacing between CMOS and TTL **05**

(b) Convert **T** flip-flop to **D** flip-flop **05**

(c) XC 4000 FPGA architecture block diagram **05**

(d) Draw truth table and logic diagram of Full subtractor **05**

Q 2 (a) Write a VHDL code for Full adder **10**

(b) Design MOD 10 asynchronous counter. **10**

Q 3 (a) Design a mealy sequence detector to detect ---1010--- using D flip-flops and logic gates **10**

(b) Design a circuit with optimum utilization of PLA to implement the following functions **10**

$R = \sum m (0, 2, 5, 7, 11, 12)$

$P = \sum m (1, 3, 8, 9, 11, 13)$

$Q = \sum m (0, 5, 8, 12, 14)$

Q 4 (a) Implement following function using 8:1 MUX and logic gates **10**

$P(X,Y,Z,W) = \sum m (0,3,4,7,8,9,13,14)$

(b) Eliminate redundant states and draw reduced state diagram **10**

PS	NS		O/P
	X=0	X=1	Y
A	B	C	1
B	D	C	0
C	F	E	0
D	E	B	1
E	B	C	1
F	C	E	0
G	F	G	0

Q 5 (a) Use K-map to reduce following function and then implement it by NOR gates. **10**

$F = \pi M (0, 3, 4, 5, 8, 10, 12, 14) + d (2, 9)$

(b) Design 8 bit up counter using IC 74163, draw a circuit diagram and explain its working. **10**

6. Write short notes on any **three** **20**

i) Noise Margins

ii) JTAG and BIST

iii) PAL and PLA

iv) Stuck at '0' and '1' faults

GN-Con.:9117-14.