SE (ETRX) SEM: III (CBSGS) NOV - DEC 2013

D. C. D.
4/12/13

25-11-2013-DTP-P-7-RA-10

Con. 9591-13. **GX - 12110**

(3 Hours) **[Total Marks :80**

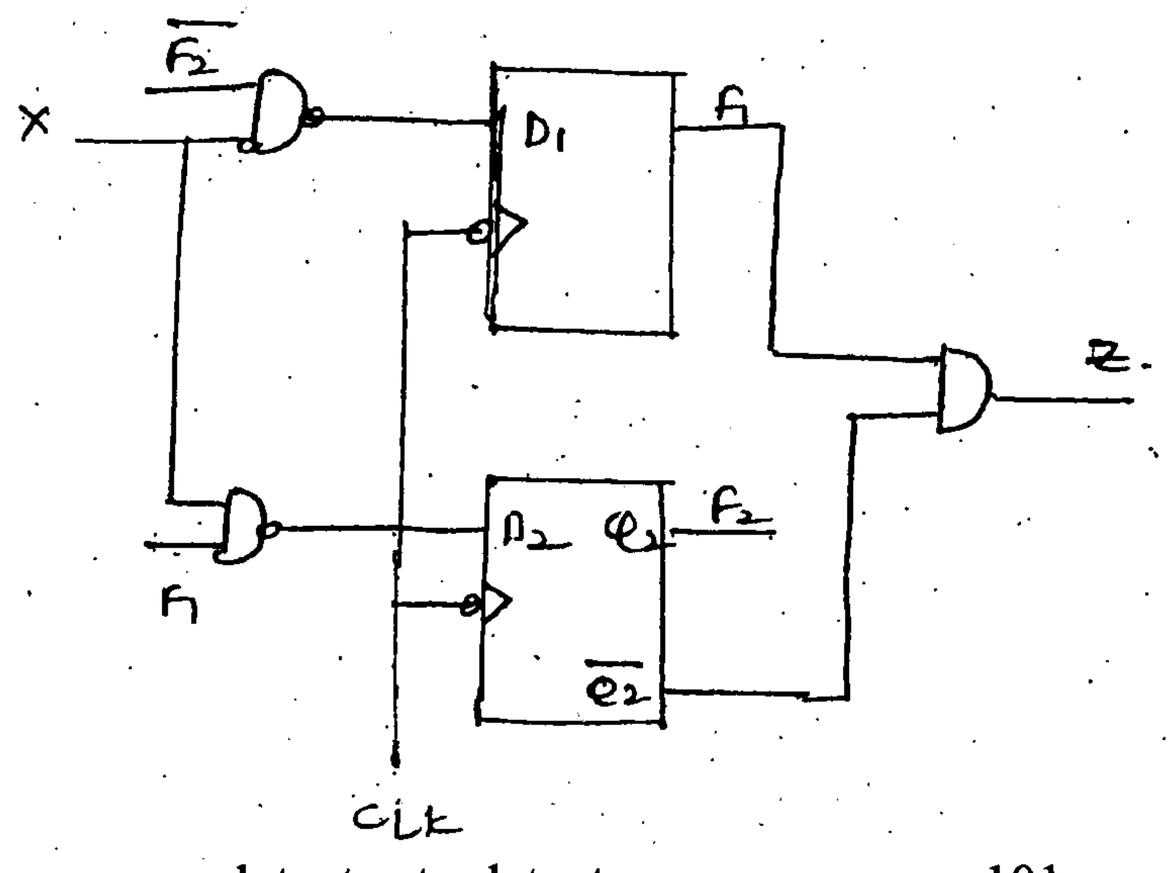
N. B. : (1) Question No. **1** is **compulsory**.
(2) Solve any **three** questions from remaining **five** questions.
(3) Draw neat **diagrams** wherever **necessary.**
(4) Furnish neat **sketches** and assume **suitable data** if required.

1. (a) Explain Moore and Mealy type of sequential circuits. **5**
(b) Draw the circuit diagram of 2-input TTL NAND gate. **5**
(c) Explain the term noise margin and its value for TTL and CMOS family. **5**
(d) Explain stuck at '0' and stuck at '1' faults. **5**

2. (a) Draw the circuit diagram of J-K F/F using NAND gates. Derive it's characteristic equation and excitation table. What is race around condition in J-K F/F and how it is avoided ? **10**
(b) Design and explain 8 bit binary adder using IC 7483. **10**

3. (a) Implement following functions using NAND gate only : **10**
(i) $F = \Sigma m (1, 2, 3, 4, 7, 11, 13) + d (9, 15)$
(ii) $F = \pi M (4, 5, 6, 7, 8, 12) + d (1, 2, 3)$

(b) Analyze the sequential state machine shown in **fig.** obtain the state diagram for the same. **10**



4. (a) Design Moore sequence detector to detect a sequence ------101------ using D F/F. **10**
(b) Discuss XC 4000 FPGA architecture with neat block diagram. **10**

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5. (a) Construct ring counter using IC 74194 and draw the output waveform. **10**

   (b) Identify indistinguishable states in the following state table and obtain minimized state diagram **10**

PS	NS		OIP	
	X = o	X = 1	X = o	X = 1
1	2	3	0	0
2	2	4	0	0
3	2	3	0	0
4	5	3	0	0
5	2	6	0	1
6	5	3	0	0

6. Write a short notes on any **three** : – **20**

   (a) JTAG and BIST

   (b) VHDL

   (c) PAL AND PLA

   (d) XC 9500 CPLD family.
