SE/Sem III/CBCS/ETRX/DCD/07-12-2017

Q. P. Code: 27584

Time: 3 Hours **Marks: 80**

N.B.: 1. Question No. 1 is compulsory.
2. Attempt any three questions out of remaining five questions.
3. Figures to the right indicate full marks.
4. Assume suitable data if required and mention it in answer sheet.

Q1. Solve following **(20 Marks)**

a) Explain the following decimals in gray code form
1. $(42)_{10}$ 2. $(17)_{10}$

b) Explain characteristics of logic families

c) State and Prove Demorgan Theorem

d) Convert JK flip flop to T flip flop.

Q2. a) What is shift register? Explain any one type of shift register. Give its applications. **(10 Marks)**

b) Implement the following Boolean function using 8:1 multiplexer.
$F(A,B,C,D)=\sum M(0,1,4,5,6,8,10,12,13)$ **(10 Marks)**

Q3. a) Explain the Johnson's Counter. Design for initial state 0110. From initial state explain and draw all possible states. **(10 Marks)**

b) Minimize the following expression using Quine McClusky technique.
$F(A,B,C,D)=\sum M(0,1,2,3,5,7,9,11)$ **(10 Marks)**

Q4. a) Design a 2 bit comparator and implement using logic gates **(10 Marks)**

b) Using Boolean Algebra and De-Morgan's theorem prove that
$\overline{Y}\,\overline{Z}+\overline{W}\,\overline{X}\,\overline{Z}+\overline{W}XY\overline{Z}+WY\overline{Z}=Z$
Simplify the expression $[A\overline{B}(C+BD)+\overline{A}\,\overline{B}]C$ as much as possible **(10 Marks)**

Q5. a) Explain the working of 3 bit asynchronous counter with proper timing diagram **(10 Marks)**

b) Design BCD Adder using the integrated circuit 4 bit binary adders. **(10 Marks)**

Q6. Write short notes on following **(20 Marks)**
a) Hazards
b) Hamming Code
c) Encoder and Decoder
d) Compare TTL and CMOS logic families

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