 40+34+02

SE Comp. IV CBSGS 25.5.17

86

Q.P. Code :13085

[Time: Three Hours] **[Marks:80]**

Please check whether you have got the right question paper.

N.B:
1. Question no 1 is compulsory.
2. Attempt any three questions from remaining five questions.
3. Assume suitable data if required.
4. Draw neat diagram wherever necessary.

Q.1 Solve any four out of five. 20

A. Explain Virtual Memory.

B. What is IO buffering?

C. Write a note on scanner.

D. What is Segmentation?

E. What is TLB?

Q.2 A. I) Draw the flow chart for Restore Division Algorithm. 04

II) Divide using restore division method 7/3. 06

B. Describe hard-wire control unit and specify its advantages. 10

Q.3 A. Multiply (-5) and (2) using Booth's Algorithm. 10

B. A block set associative cache consists of 64 blocks divided in 4 block sets. The main memory contains 4096 blocks, each 128 words of 16bit length. 10

1) How many bits are there in main memory address?

2) How many bits are there in cache memory address (tag, set, and word fields)?

Q.4 A. Differentiate between I. RISC and CISC processor. 10

B. Explain Flynn's classification. 10

Q.5 A. Discuss the functions of 8089 I/O processor. 10

B. Show IEEE 754 standards for Binary Floating Point Representation for 32 bit single format and 64 bit double format. 10

Q.6 A. Explain different pipelining hazards. 10

DMA

B. Discuss the functions of 8089 I/O processor 10

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