(3Hrs) Max Marks: 80

NB: 1. Question No.1 Compulsory.
2. Solve any THREE from Q.2 to Q.6
3. Assume suitable data whenever necessary with justification.

Q1. Answer any four questions

	(A)	Explain Instruction and Instruction Cycle.	(05)
	(B)	Explain Booths algorithm with an example	(05)
	(C)	Give different instruction formats.	(05)
	(D)	Describe the memory hierarchy in the computer system	(05)
	(E)	Explain Superscalar Architecture.	(05)
Q2.	(A)	Explain Branch Predication Logic and delayed branch.	(10)
	(B)	List and explain various data dependencies, data and branch hazards that occur in the computer system.	(10)
Q3.	(A)	A program having 10 instructions (without Branch and Call instructions) is executed on non-pipeline and pipeline processors. All instructions are of same length and having 4 pipeline stages and time required to each stage is 1nsec. i) Calculate time required to execute the program on Non-pipeline and Pipeline processor. ii) Calculate Speedup	(10)
	(B)	What is Microprogram? Write microprogram for following operations. i) ADD R1, M, Register R1 and Memory location M are added and result store at Register R1. ii) MUL R1, R2 Register R1 and Register R2 are multiplied and result store at Register R1.	(10)
Q4.	(A)	Explain Bus Contention and different method to resolve it.	(10)
	(B)	Describe memory segmentation in detail. Explain how address translation is performed in virtual memory.	(10)
Q5.	(A)	State the various types of data transfer techniques. Explain DMA in detail.	(10)
	(B)	Consider a cache memory of 16 words. Each block consists of 4 words. Size of the main memory is 256 bytes. Draw associative mapping and calculate TAG, and WORD size.	(10)
Q6.	(A)	Write short note on Performance measures	(10)
	(B)	Draw and explain floating point addition subtraction algorithm.	(10)

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