Q.P. Code : 541001

(3 Hours) **[Total Marks : 80]**

N.B. 1) Question number 1 is compulsory.
2) Attempt any 3 questions from the remaining 5 questions.
3) Each question carries 20 marks.
4) Within a question, each sub-question carries equal marks.

1. a) Convert $(-124)_{10}$ to its equivalent sign magnitude form. **02**
b) Convert decimal 214.32 into base 7. **02**
c) Add $(7)_{10}$ and $(6)_{10}$ in BCD **02**
d) Simplify (B+A)(B+D)(A+C)(C+D). **02**
e) Construct Hamming code for BCD 0110.Use even parity. **02**
f) Prove that "A positive logic AND operation is equivalent to a negative logic OR operation". **02**
g) List the applications of shift registers. **02**
h) Minimize the following standard POS expression using K-map **03**
$Y = \Pi M(0,2,3,5,7)$
i) Write the entity declaration construct in VHDL for NOR gate. **03**

2. a) Obtain the minimal expression using Quine-Mc Cluskey method. **10**
$F(A,B,C,D) = \Sigma m\,(1,5,6,12,13,14) + d(2,4)$
b) Compare TIL, CMOS and ECL families with respect to gate, voltage level, fan-in, fan-out, propagation delay, power dissipation, speed and noise margin. **10**

3. a) Design a logic circuit to convert BCD to Gray code. **10**
b) Implement the following using 8:1 MUX. **05**
$F(A,B,C,D) = \Sigma m\,(0,1,3,5,7,10,11,13,14,15)$
c) Explain Astable multivibrator. **05**

4 a) Explain Master-Slave J-K flipflop. **05**
b) Design 1:16 Demultiplexer using 1:4 demultiplexer. **05**
c) Explain Data flow modelling and Behavioural modelling in VHDL. **10**

(TURN OVER)

5. a) Convert JK flipflop to SR flipflop and D flipflop. **10**
   b) Design mod 12 asynchronous UP counter. **10**

6. **Write short note on (any four):-**
   a) Ring Counter
   b) State table
   c) 2-bit Magnitude comparator
   d) 3 to 8 line decoder
   e) Universal shift register

****