SE / CMPN / III CBGS
PLDA
3/6/2014.

QP Code : NP-18720

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Solve any **three** questions from **remaining**.
(3) **Figures** to the **right** indicate **full** marks.
(4) Assume **suitable** data if **necessary**.

1. (a) Perform following without converting into other bases. **5**
   (i) $(57)_8 * (24)_8$ (ii) $(312{\cdot}0)_4 + (213{\cdot}2)_4$
   (b) Define following Parameters for CMOS family :— **5**
   (i) Fan out (ii) Fan in.
   (c) Design a full adder using half adder and additional gates. **5**
   (d) Explain concept of bistable multivibrators. **5**

2. (a) Using Quine MC Clusky method determine minimal SOP form for : **10**
   $F(A, B, C, D) = \Sigma m\ (1, 2, 3, 6, 7, 10, 12, 14)$
   (b) Obtain even Parity hamming code for 1010. Prove that hamming code is an error detecting and correcting code. **10**

3. (a) Explain the operation of 4-bit universal shift register. **10**
   (b) Design a 2-bit digital comparator that accepts inputs A and B and gives three outputs G, E and L. **10**
   (i) Output G, when A > B
   (ii) Output E, when A = B
   (iii) Output L, when A < B.

4. (a) Implement the following using 8:1 Mux. **10**
   $F(A, B, C, D) = \pi M(1, 3, 5, 9, 11, 12, 13)$.
   (b) Simplify following function using k-map. **10**
   $F(A, B, C, D) = \Sigma m\ (1, 2, 3, 4, 6, 8, 10, 14, 15)$

5. (a) Design a sequence generator for following sequence. Identify and check for lock out condition **10**
   $0 \rightarrow 3 \rightarrow 5 \rightarrow 6 \rightarrow 0$.
   (b) Explain 4-bit Johnson counter. Draw its timing diagram. **10**

6. Attempt any **two** :— **20**
   (a) Working of Master-Slave J-K flip flop.
   (b) Details and comparison of FPGA and CPLD.
   (c) Convert the following :—
   (i) SR to JK (iii) JK to D
   (ii) SR to D (iv) JK to SR.