Sem. III (CMPN) (CBCS) (DLDA) Dec.17

29/11/17

Q.P. Code: 24869

(3 Hours) **[Max. Marks 80]**

N.B. (1) Question No. 1 is compulsory
(2)Assume suitable data if necessary
(3)Attempt any three questions from remaining questions

1

(a) Convert $(1762.46)_{10}$ into octal, binary and hexadecimal. **(3)**

(b) Prove OR-AND configuration is equivalent to NOR-NOR configuration. **(3)**

(c) Perform Subtraction using 16's complement. **(4)**
i) $(CB1)_{16} - (971)_{16}$
ii) $(426)_{16} - (DBA)_{16}$

(d) Find 8's complement of following numbers. **(2)**
i) $(27)_8$ ii) $(321)_8$

(e) Perform following subtraction $(52)_{10} - (65)_{10}$ using 2's complement method. **(2)**

(f) Write the hamming code for 1010. **(2)**

(g) Implement the following Boolean equation using NAND gates only. **(2)**
Y = AB + CDE + F

(h) Explain the term prime implicant. **(2)**

2 (a) Design a 4-bit ripple adder. **(10)**

(b) Obtain the minimal expression using Quine Mc-Cluskey method **(10)**
F(A,B,C,D) = ∑m (1, 5,6,12,13,14) + d(2,4,)

3 (a) Implement a full adder using 8: 1 multiplexer. **(10)**

(b) Implement the following functions using demultiplexer. **(5)**
F1 (A, B, C) = ∑m (0, 3, 7) F2 (A, B, C) = ∑m (1, 2, 5)

(c) Simplify F (A, B, C, D) =∏M (3, 4, 5, 6, 7, 10, 11, 15) and implement using minimum number of gates. **(5)**

4 (a) Compare TTL and CMOS logic with respect to fan in, fan out, propagation delay, power consumption, noise margin, current and voltage parameters. **(5)**

(b) Draw the circuit for S-R flip flop using two NOR gates and write the architecture body for the same using structural modelling. **(5)**

(c) Explain 1-digit BCD Adder. **(10)**

5 (a) Convert JK flip flop to SR flip flop and D flip flop. **(10)**

(b) Design 3 bit synchronous counter using T flip flops. **(10)**

6 Write short note on **(any four)** **(20)**
(a) State table
(b) ALU IC 74181
(c) Sequence Generator
(d) Data flow modelling
(e) 4-bit ring counter

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